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R&D EQUIPMENT INFORMATION REPORT
Time Lapse Storage System

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Equipment is described which stores and plays back data obtained by a coherent meteorological radar. The Time Lapse Storage System (TLS) operates in two modes, Acquire and Recall. Acquire facilitates the transfer of up to 400 sets of data from four color CRT displays to an 80 megabyte disc, either at user specified intervals or at the end of each antenna scan. During Recall, sets of data are transferred from the 80 megabyte disc to the displays. The user specifies which sets of data he wishes to view and the length of real time display for each set in order to visually track the progress of storm cells.

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SECTION 1. INTRODUCTION

The SCRM (Scan Converter/Refresh Memory), in combination with a suitable radar and signal processing system, has been a useful tool for the radar meteorologist. Its memory capacity, however, is inadequate to permit detailed study of the time-varying structure of meteorological phenomena. It can store four images manually-captured at different times; however, a detailed comparison among them is difficult because they appear in different displays. In addition, this mode of operation compromises the display of more than one variable or the use of the CAPPI (Constant Altitude Plan Position Indicator) display mode.

This equipment information report describes a TLS (Time Lapse Storage) system, based on a large rotating magnetic mass memory, which expands the memory capacity of the SCRM by more than two orders of magnitude. The TLS periodically acquires sets of images from the SCRM during normal system operation. Later, the TLS can be directed to enter the recall mode in which sets of images, addressed either by time of storage or set number, can be recalled to the SCRM's displays in a variety of manual or automatic forward or reverse sequences.

SECTION 2. GENERAL DESCRIPTION

The heart of the TLS is a large magnetic disc mass storage unit. Because discs are invariably designed with controllers compatible with some processor, the most economical and flexible implementation for the TLS includes a small processor, even though the required performance could certainly be achieved with a special purpose hardware design. The following section describes the hardware configuration of the TLS and how it fits into the SCRM, while the last section gives a general description of how the TLS is used and what level of performance it can achieve.

2.1 System Configuration

A block diagram of the TLS is presented as Figure 2-1. The 6/16 processor chassis, containing the processor itself, 32K bytes of 1 microsecond core memory for program storage and data buffering, and the various peripheral controllers, is mounted in the SCRM cabinet below the DISPLAY INTERFACE CONTROL panel. The MODEM, formerly located in this position, has been relocated since easy access to it is not mandatory. The power supply for the 6/16 processor chassis is located behind the chassis, mounted from the rear of the cabinet.

As described in later sections, the SCRM's DDI card requires modifications to interface it with the TLI (Time Lapse Interface) circuitry, added to the MAG card in the SCAN CONVERSION PROCESSOR chassis. The TLI is designed to communicate with special hardware added to a ULIM (Universal Logic Interface Module) which plugs into the 6/16's SELCH (Selector Channel) bus. The resulting interface allows block transfers of image data in either direction between the SCRM image memories and 16K bytes of the 6/16 core memory set aside as a buffer. These transfers, accomplished by means of a cycle-stealing direct-memory-access process, can reach transfer rates of up to 2×10^6 bytes/second but are limited to slightly lower rates by SCRM limitations discussed in later sections.

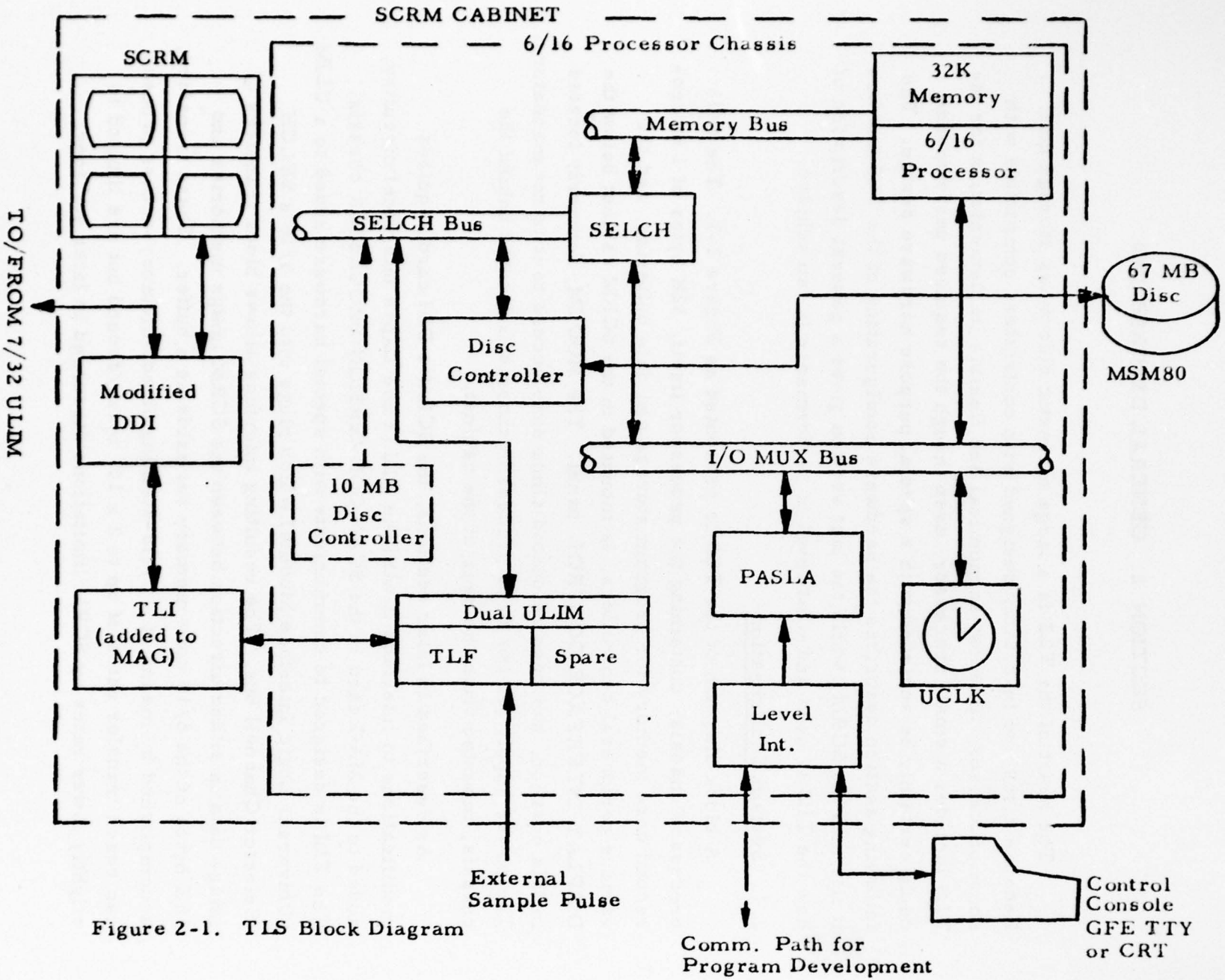


Figure 2-1. TLS Block Diagram

The contents of the 16KB buffer are transferred to or from the disc, an MSM80 Removeable Media Mass Storage Module, via a two-card disc controller also connected to the SELCH bus. The buffer capacity exactly corresponds to that of one track of the disc, thus a block transfer can be achieved in one rotation period or 16.7 milliseconds, with a peak transfer rate of 1.2×10^6 bytes/second. The formatted capacity of the removeable disc pack is 67,420,160 bytes, or 823 five-track cylinders of 81,920 bytes each. Each SCRM image requires 320 x 256 x 4 bits or 40,960 bytes with two pixels per byte. Thus, 2.5 tracks are needed per image and 2 cylinders can contain an entire set of four images. Storage of over 400 sets of images is thus possible in the MSM80.

An External Sample Pulse input is provided so that the acquisition of sets of images can be synchronized with external processes such as antenna scanning. This pulse generates an interrupt in the ULIM. Internal timing is developed by a programmable Universal Clock module.

Control of the TLS is accomplished through a GFE Control Console which can be either a teletype machine or a CRT terminal. A PASLA (Programmable Asynchronous Line Adapter) interfaces the console with the 6/16 and also allows interprocessor communication useful in software development.

2.2 Operational Capabilities

In addition to the 400-set storage capacity, there are time limitations on the block transfers between memories. These arise from transfer rate and synchronization-time bounds and are 620 milliseconds per set of images going to the disc, and 850 milliseconds per set of images being recalled. These times include rotational latency and head relocation of the disc drive. The transfer times have been made as fast as possible without extensive SCRM hardware changes in order to avoid both ambiguities in acquisition of changing images and annoying visual effects during recall. The transfer sequence has been designed so that the radar data area of each image (2 tracks) changes in only 167 milliseconds during recall.

The operator controls the TLS through the control console keyboard by means of simple command sequences which specify the desired operating mode and parameters. In the Acquisition mode, the operator can select any sampling interval up to 60 minutes, in one second increments, in order to match a wide range of radar scan rates or modes. At each sampling time, the contents of all four SCRM image memories are automatically stored on the disc. The time, in a DAY:HR:MIN format, is recorded separately for each set of images. An External Sample Pulse input is provided so that sampling times can be synchronized with antenna scanning sequences if desired. One application of this feature would be in acquiring a series of CAPPI presentations by triggering the TLS at the end of each elevation scan.

Acquisition can also be programmed to stop at a certain image set number, or to over-write the oldest data sets. More than one sequence can be acquired by specifying appropriate starting and ending set numbers.

The Recall mode offers the operator a wide variety of display sequences made possible by the access properties of the disc memory. Automatic sequential playback either forward or backward in time is possible with display times ranging between one and 60 seconds per image. Any number of contiguous sets of images can be indefinitely cyclically repeated for detailed study. Manual incremental access in either direction is possible. Random-access is achieved by operator entry of the DAY:HR:MIN time desired; the TLS subsequently finds and displays the image set having the closest time to that just entered. From this starting point, any of the automatic or manual display sequences can proceed.

In some cases, it may be desired to retain one or more of the SCRM image memories for other applications. For this reason, the TLS includes independent "Playback Enable" controls for each of the four display channels.

Acquisition and recall are not mutually exclusive. If the acquisition sampling interval is greater than the time for one antenna scan, then the remaining time can be used for recall. The basic timing for this scheme is illustrated in Figure 2-2, where the "sample pulse" is generated either

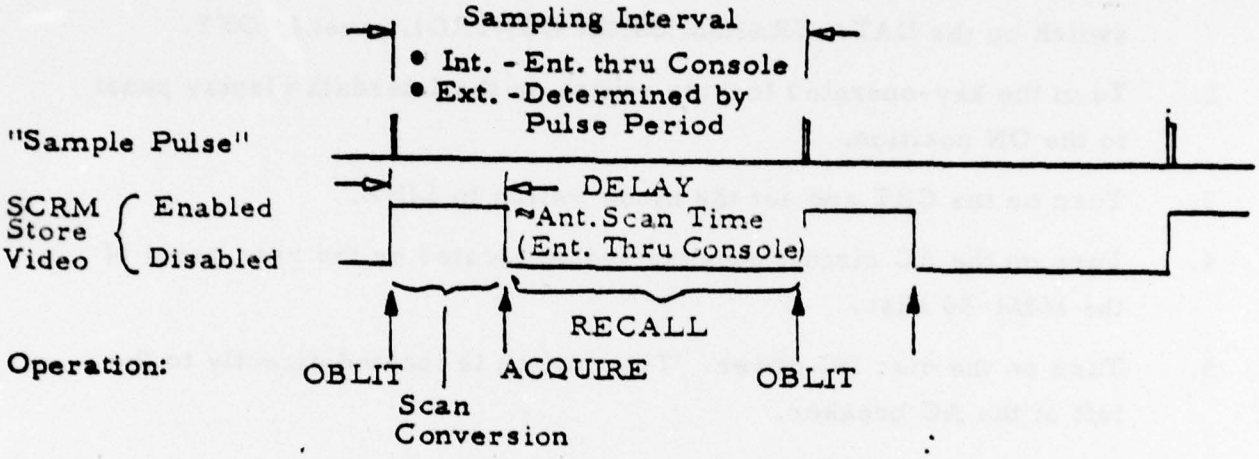


Figure 2-2. Acquire During Recall Timing

internally by software with period specified by the user through the console, or externally by a pulse which generates an interrupt through the TLI. The radar data areas of all selectal display channels are erased at this time by a subroutine called OBLIT so that range or altitude markers stored as color 15 will not "show through" the newly scan-converted images. In this mode the user must also specify a DELAY time, equal to or slightly greater than the time for one antenna scan, to allow for the scan conversion process to take place in the SCRM in the normal way. After this delay, further "Store Video" operations in the scan converter are inhibited in all display channels previously selected for recall. The current set of images is then acquired by the TLS which then enters its recall mode which can continue under normal operator control until the next sample pulse.

SECTION 3. OPERATION

3.1 System Startup and Shutdown

Assuming that the command console is a CRT terminal, following these ten steps will ready the system for operation:

1. Make sure the scan converter power switch is ON and the MODE switch on the DATA TRANSMISSION CONTROL panel is OFF.
2. Turn the key-operated locking switch on the Interdata display panel to the ON position.
3. Turn on the CRT and set the mode switch to LINE.
4. Turn on the AC circuit breaker switch located on the rear panel of the MSM-80 Disc.
5. Turn on the disc DC power. This switch is located directly to the left of the AC breaker.
6. Depress the START button on the front of the disc.
7. Watch the disc READY light. When it stops flashing and remains stable, you may proceed to the next step.
8. Depress the DTA button on the Interdata display panel.
9. Depress 4, 0 and 0 again.
10. Depress ADD, INI, and then RUN. The system will reply with a message and a prompt (*) to the CRT.
11. OPTIONAL: Enter the system test command TEST through the CRT to ensure that the above steps were carried out properly. If system test fails, repeat above procedure before suspecting a system failure.

The system will now respond to CRT input.

CAUTION: The MSM-80 Disc must be treated with extreme care. Please refer to Interdata's Publication Number 29-512, "MSM Removable Cartridge Disc System Maintenance Manual" for full installation and operation details.

NOTE:

If it becomes apparent the system has become hung up while operating; that is, it will not accept or react to any commands; it is not necessary to repeat the entire turn-on procedure. Merely:

1. Depress SGL button on Interdata display.
2. Repeat from Step 7 of the Turn-on procedure.

Following these steps will safely shut down the system:

1. Enter the STOP command through CRT.
2. Depress SGL.
3. Depress the START button on the front of the disc.
4. Watch the disc READY light. When it stops flashing and remains stable, you may proceed to the next step.
5. Turn the DC power switch on the rear of the disc to OFF.
6. Turn OFF the neighboring AC circuit breaker.
7. Turn OFF the CRT.
8. Turn the key-operated locking switch on the Interdata display panel to the OFF position.

3.1.1 Reloading the System

Facilities have been provided to save the system program on the MSM-80 Disc, so that it can be easily reloaded if for any reason core is wiped out. The procedure is as follows:

1. Be sure the disc and 6/16 are ON and ready.
2. Load memory locations as follows:

Addr	Contents	Press:
007A	FC35	DTA 7A ADD
007C	FBF0	DTA FC35 WRT
007E	0111	DTA FBF0 WRT
		DTA 111 WRT

3. The three-position Autoload switch is edge mounted on the right side of the second board from the top of the 6/16 chassis. It is normally in the DIS position (extreme left). Move it to the center position.

4. Depress INI on the console. The system will be reloaded and automatically started.

5. Move the Autoload switch back to the extreme left position.

3.2 TLS Commands

Table 3-1 summarizes what commands the TLS Command Processor will accept and describes in detail the actions each command initiates. When specifying a recall or acquire sequence, bear in mind that the disc set numbers are treated on a modulo 400 basis.

3.2.1 Recall

It is advisable to input an SDC command before specifying a recall sequence because system startups and STOP commands clear any previously selected display channels. If the user neglects to select display channels, TLS still enters the Recall mode but will not write to the screens until displays are selected. The system would not suffer, but unnecessary confusion would probably result when the user realizes the sequence he specified does not appear to be in progress. Also, note that the sequence will begin at the specified starting set no matter how long the user delays before entering an SDC command.

3.2.2 Acquire

Almost everything the user needs to know about Acquire is contained in Figure 2-2 and Table 3-1. The need for obliterating the screens vanishes if the user does not plan on specifying a recall sequence during Acquire. In order to prevent this potential annoyance from happening, enter STOP or SDC Carriage Return before inputting an acquire command; however, a non-zero delay time must still be included in the command.

TABLE 3-1 TLS Command Grammar

Command	Functional Description	Examples
SDCwxyz	Select Display Channels: The SCRM display channels desired for recall are specified. $1 \leq (w, x, y, z) \leq 4$	SDC234
Am:n;Dt;Se, f, gc	Acquire a set of images every m minutes and n seconds, allowing t seconds of real-time display on the SCRM, beginning with set number e, in increments of g sets, until f sets have been stored. If c is C, cyclically write over set e, e+g, etc., as new sets of images are acquired. If g is omitted, assume it is 1. Restrictions: $1 \leq (e, f) \leq 400$ $0 \leq m \leq 60$ (1 of 2 digits) $0 \leq n \leq 60$ (2 digits) $1 \leq t \leq 99$ c = blank or C If C is not present: $60\,m + n > t$ (delay cannot exceed sampling interval) $-99 \leq g \leq 999$ If C is present: $-9 \leq g \leq 99$	A4:00; D57; S131, 100,C A0:59; D50; S131, 100 A4:30; D50; S131, 100, -9C
AE;Dt; Se, f, gc	Acquire a set of images every external sample pulse allowing t seconds . . . . etc., as above.	AE;D60;S9, 301, 2
Rs;Si, j, kp	Recall a set of images every s seconds beginning with set no. i, in increments of k sets, until j sets have been recalled. If p is blank, stop. If p is C, cyclically repeat display of sets i through i + j. If k is omitted, assume it is 1. $1 \leq (i, j) \leq 400$ $1 \leq s \leq 60$ p = blank or C If C is not present: $-99 \leq g \leq 999$ If C is present: $-g \leq g \leq 99$	R20;S56, 300, 3C

TABLE 3-1 (Continued) TLS Command Grammar

Command	Functional Description	Examples
Rs; Td:h:b, j, kp	Recall a set of images every s seconds, beginning with the set having time closest to d(day); h(hours); b(minutes), in increments of k sets, until . . . etc., as above.	R16;T150:19:08, 36, C R16;T150:19:08, 36, 2C
	$0 \leq d \leq 999$ days, $0 \leq h \leq 24$ hours, $0 \leq b$	<60 minutes.
RIn	Recall the set having number n greater than the one being displayed. $1 \leq n \leq 99$. If n is omitted, assume it is 1.	RI
RDn	Recall the set having number n less than the one being displayed. $1 \leq n \leq 99$. If n is omitted, assume it is 1.	RD2
TEST	Activate System Test	TEST

3.2.3 Recall During Acquire

The timing of operations occurring during this mode is depicted in Figure 2-2. During the delay interval, recall sequences are merely suspended--they are not terminated. The sequence will continue from where it was suspended when the delay interval ends. The user should be aware that an OBLIT signals the beginning of the delay period. Recall's cyclical output option should be avoided in this mode, because the user will not be able to halt Recall without also stopping Acquire (STOP command stops both). The user should enter SDC Carriage Return as described in Section 3.2.2 after the recall sequence ends and the last recording has been obliterated, if he does not plan on entering another recall command shortly.

3.2.4 Storing Thresholds

The tedium of storing a set of thresholds onto the displays has long disturbed SCRM users. If allocating a few sets exclusively to threshold storage does not present a problem, TLS may be used to simplify the task somewhat. Commonly used thresholds should be stored in reserved sets specified by the user. When a particular set of thresholds is desired, follow these steps:

1. Depress the blue ERASE DISPLAY buttons on the DISPLAY INTERFACE CONTROL panel.
2. Depress the STORE THRESHOLDS buttons on the SCAN CONVERSION PROCESSOR panel.
3. Recall the set of desired thresholds.

3.2.5 External Sample Pulse

The external sample pulse is a TTL level signal which goes low when an acquisition is desired. This signal is to be applied to the BNC connector mounted on the TLF and facing the front panel. The pulse may be of any duration greater than 100 ns and less than 1 μs.

SECTION 4. DETAILED HARDWARE DESCRIPTION

The interface between the SCRM and the TLS 6/16 Control Sequencer consists of the Time Lapse Formatter (TLF), contained on a Universal Logic Interface Module plugged into the 6/16 chassis, and Time Lapse Interface (TLI) logic which was added to the Memory Address Generator (MAG) wire-wrap panel in the SCRM. The TLF interfaces with the 6/16 control and memory bus. Interconnection between the two locations requires a ten foot cable carrying 23 active signals. To achieve error-free performance, each signal is carried on a terminated unbalanced pair in a flat ribbon cable. The cable contains 25 wire pairs and interconnects between a 50-pin connector on the TLF and two 26-pin connectors on the TLI. Two spare pairs are provided for future expansion.

4.1 TLF-TLI Interaction

The basic logic for interfacing with the 6/16 SELCH bus is supplied on the ULIM as purchased from MDB Systems, Inc. It includes data line drivers and receivers, device address decoding, interrupt circuitry, and status and interrupt gating. The ULIM also contains 92 wire wrappable sockets for IC logic designed by Raytheon hereafter referred to as the Time Lapse Formatter (TLF). A block diagram of the TLF and the TLI are shown in Figures 4-1 and 4-2. All data transfers between the SCRM and the TLS disc memory are performed via the TLF.

Data transfers from the SCRM to the TLS disc (Acquire Mode) are initiated by the 6/16 when it sends a start command (ITFR = 1 and all RE bits = 0, see Table 4-2) to the TLI via the TLF. If neither SDF Test has been selected, then SDFT = 0 and the Initiate Transfer command is accepted; ITAC goes high. If the 6/16 senses status at this time, it will find Device Unavailable (SIN7) to be false, thus it can verify that the command was accepted. Since all RE bits in the command byte are false, RECALL is low

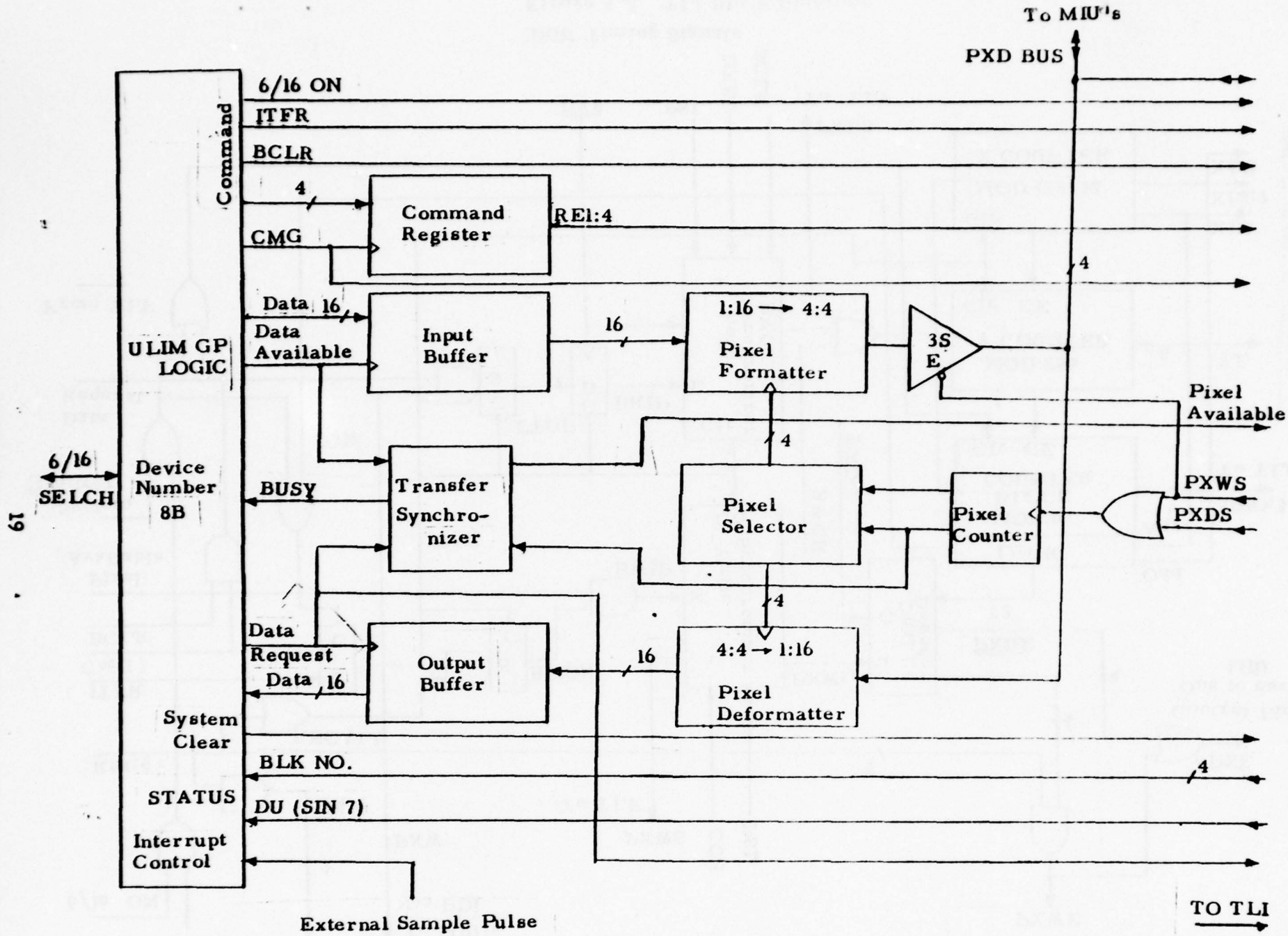


Figure 4-1 TLF Block Diagram

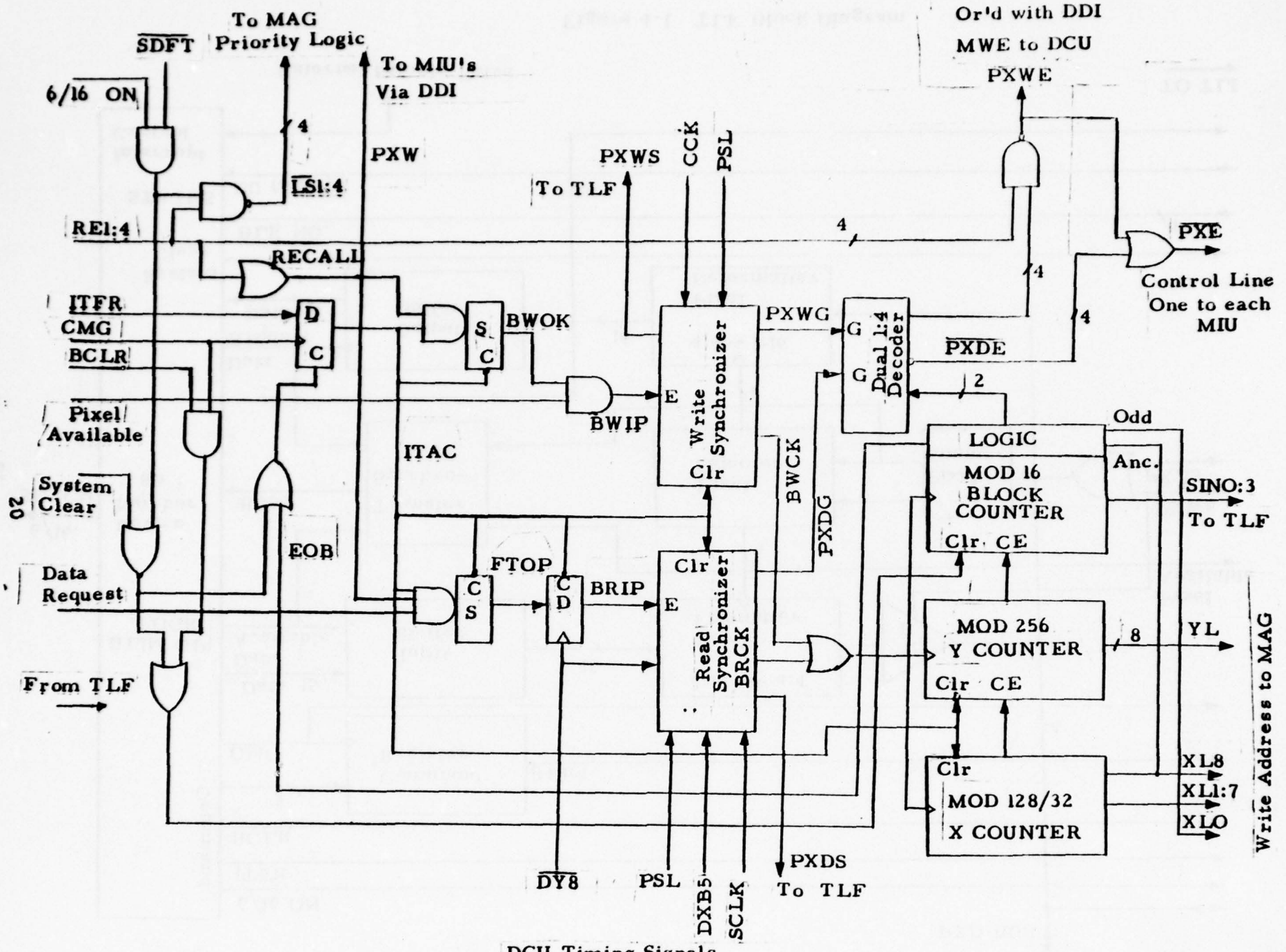


Figure 4-2 TLI Block Diagram

so that the BWOK flip-flop is not set but the FTOP flip-flop is enabled to be set when the first Data Request pulse is received through the GP logic. This first pulse indicates that the SELCH has received a GO command, has found BSY (SIN4) to be false (the buffers in the TLF are designed to start each transfer with BSY false), and has requested the first halfword of data then set BSY high. The software ignores this first halfword since it consists of the old contents of the Output Buffer.

With FTOP now true, up to 16.7 milliseconds elapses until the top of the SCRM raster scan field is reached, at which time BRIP goes high and enables the READ Synchronizer, which then generates several different timing pulses at a peak rate just under 3 MHz. BRCK is applied to the address counters since RECALL is low. PSDG becomes PXDE to capture pixel data on the particular MIU selected by the BLOCK Counter, channel one at this point in the sequence. PXDS informs the Pixel Deformatter that a pixel is arriving on the PXD BUS from the selected MIU. More will be said later about READ Synchronizer operation.

Pixel data enter the Deformatter in bursts up to 128 pixels long with a uniform rate during each burst of just under 3×10^6 pixels/sec. The Pixel Deformatter in the TLF builds a 16-bit halfword from 4 pixels. When 4 pixels have been received, the Pixel Deformatter strobes the halfword into the Output Buffer which then makes a Transfer Request to the 6/16 SELCH by setting BSY low. The 6/16 SELCH transfers the halfword into its buffer memory by issuing a Data Request strobe; meanwhile the TLI continues to transfer pixels. The 6/16 SELCH can transfer 10^6 halfwords per second, while the TLI transfers data at a peak rate of 0.75×10^6 halfwords per second. Thus the 6/16 is required to use only a maximum of 75% of its data transfer bandwidth. Transfers continue until the 6/16 SELCH has received the requisite number of data at which time it terminates the transfer process. Termination also occurs in the TLI when the address counters reach the End of a Block and EOB goes high.

Data transfers from the TLS disc to the SCRM (Recall Mode) are also initiated by the 6/16 which sends a start command (ITFR = 1 and one or more RE bits = 1, see Table 4-2) to the TLF. If SDFT = 0, then ITAC goes high which can be verified by a sense status operation by the 6/16. Since one or more RE bits, corresponding to those channels which are to display recalled images, are true, RECALL is true and the BWOK flip-flop is set while the FTOP flip-flop is not. The SELCH receives a GO command and, finding BSY low initially, issues a Data Available strobe to the Input Buffer which accepts the first halfword then sets BSY high.

The Pixel Formatter accepts the halfword from the Input Buffer and transfers pixel characters sequentially to the SCRM via the PXD BUS. Meanwhile, the Input Buffer requests the next halfword by setting BSY false and then makes it available to the Buffer/Formatter which accepts it when it has transferred its 4 pixels to the SCRM. The PIXEL AVAILABLE signal remains low until the first pixel is ready to go at the formatter output, at which time BWIP enables the WRITE Synchronizer. The Block Write operation is much simpler than the read because there is no need to synchronize to the refresh raster scan timing, only to the individual 1.67 usec SCRM memory cycles during which one pixel is written in a display channel and at an address determined by the TLI address counters. When enabled, the WRITE Synchronizer generates several different timing pulses at a peak rate just under 6×10^5 Hz. BWCK is applied to the address counters since RECALL is high. PXWG becomes PXWE to enable pixel data from the PXD BUS to the C register input in the particular MIU selected by the BLOCK Counter, channel one at this point in the sequence. PXWE control lines for channels having their RE bits low are disabled. The PXWE lines are also or'd with DDI MWE lines on the DDI; these signals travel to the SCRM's DCU card where they initiate memory read-modify-write cycles so that the pixels on the PXD BUS can be written into the appropriate image memory. PXWS clocks a pixel out of the formatter and enables it onto the PXD BUS.

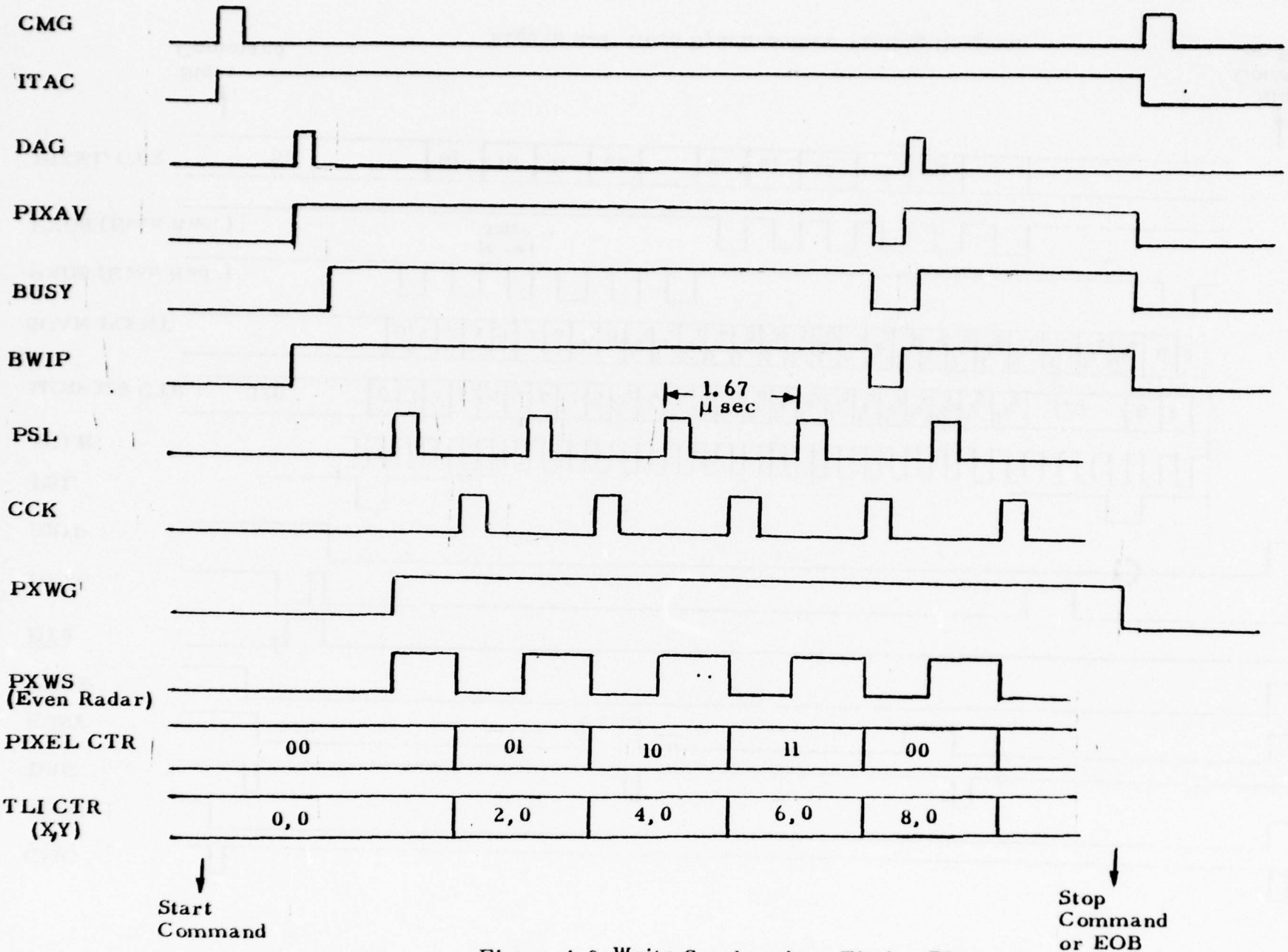


Figure 4-3 Write Synchronizer Timing Diagram

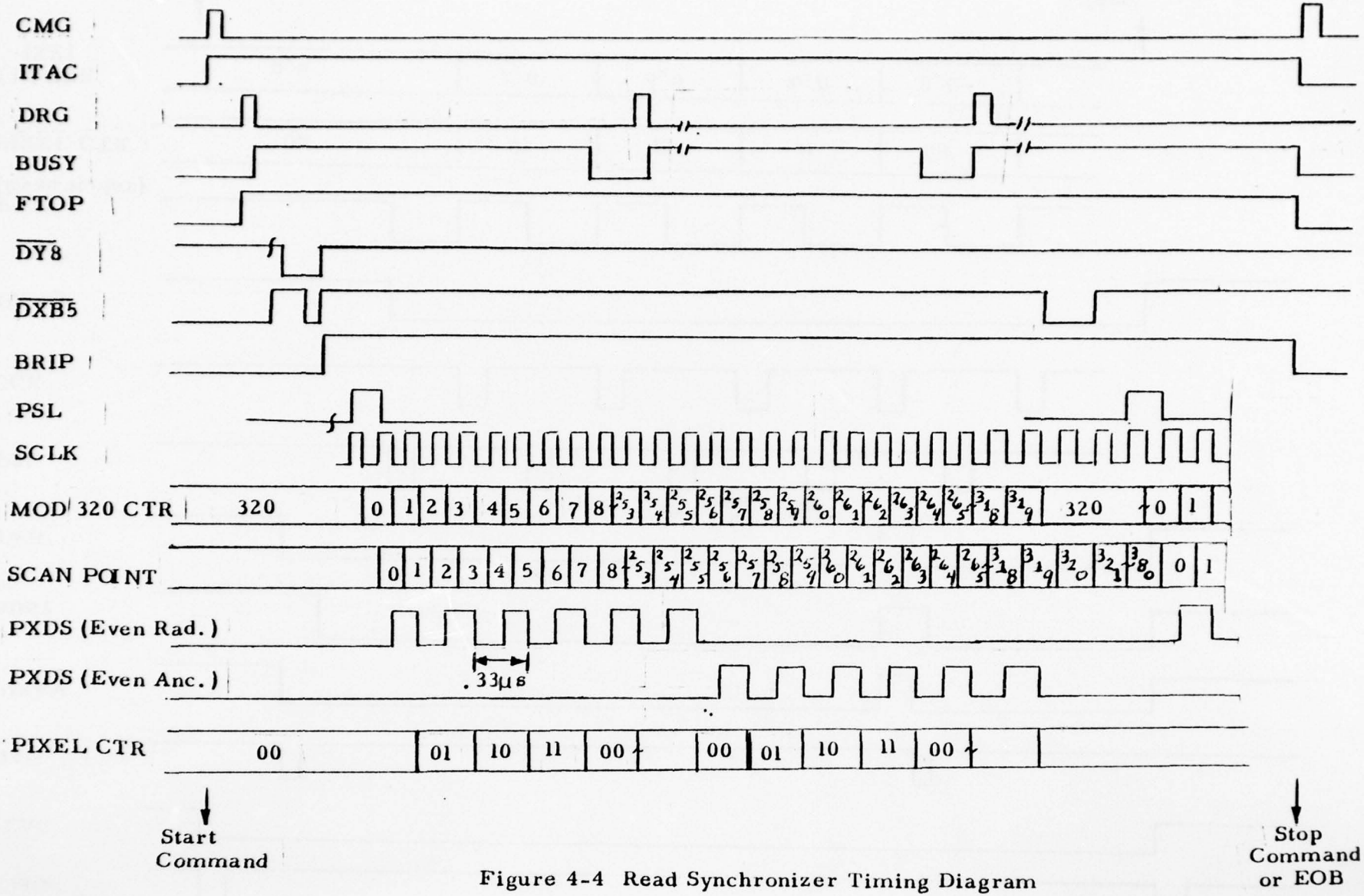


Figure 4-4 Read Synchronizer Timing Diagram

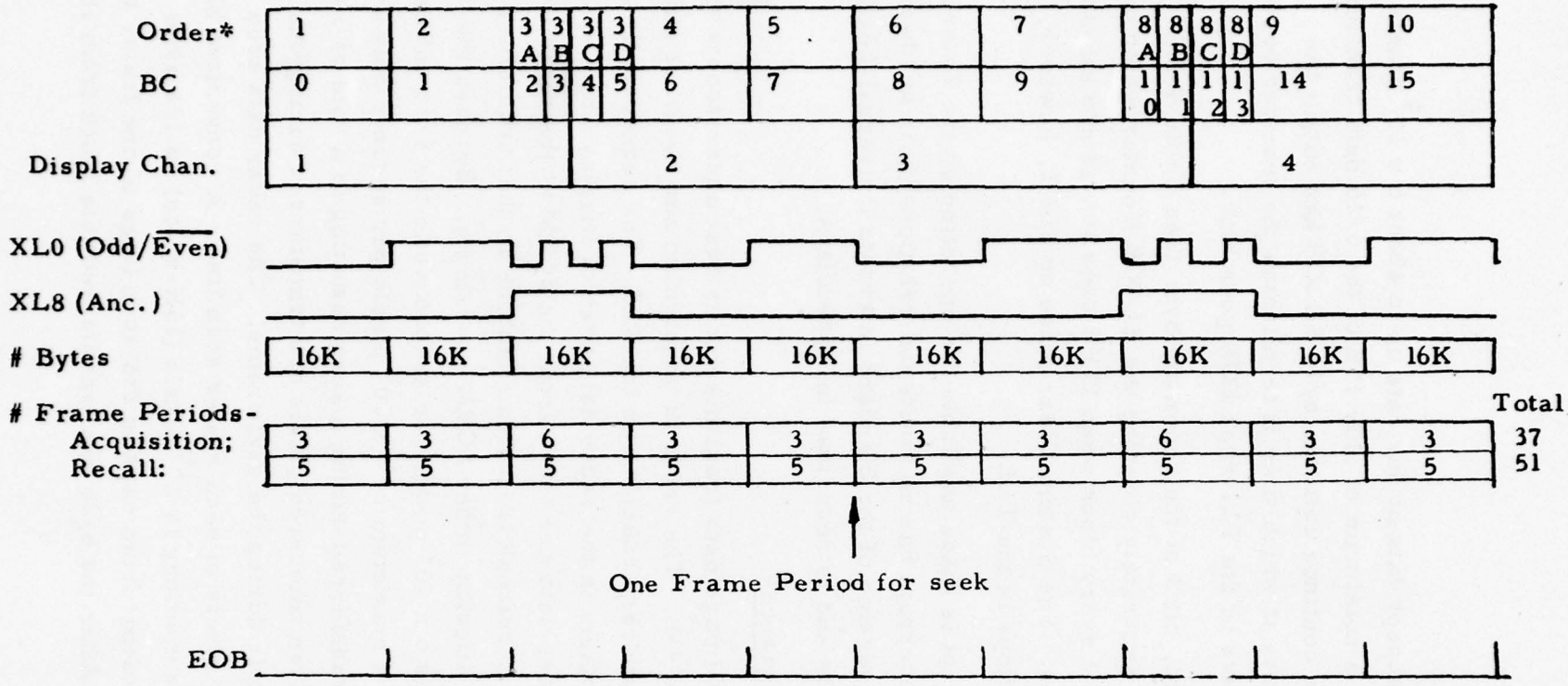
The SCRM can accept data at any rate up to about 6×10^5 pixels per second thus requiring a maximum of only 15% of the 6/16 data transfer bandwidth. Transfers continue until the 6/16 SELCH has output the requisite number of data at which time it terminates the transfer process. Termination also occurs in the TLI when EOB goes high.

The BCLR signal, bit 3 of the command byte (see Table 4-2), provides a means for separately clearing the BLOCK Counter which cannot be cleared at the end of every block when ITFR goes low as are all other counters and flip-flops. The System Clear pulse or SDFT, however, clear all counters and flip-flops in the TLI.

The TLF Interrupt is made available for operation by the External Sample Pulse. The Interrupt has no functional relationship in hardware to the TLI. A modified version of the Standard Interdata Universal Logic Module test is provided and is described in Appendix A.

4.2 TLI Address Sequence

The sequence of image data transmission is best understood with the aid of Figures 4-5 and 4-6. The order of acquisition and recall of pixels is determined by the address counters on the TLI. The sequence always begins with the even pixels in the radar data area of Display Channel One. In the Acquisition mode, data are taken from the SCRM at the same time as they are being output to refresh the video monitors so that acquisition can be accomplished without affecting other SCRM operations. Because the data rate to each monitor is 6×10^6 pixels per second while the 6/16 buffer memory can transfer a maximum of 4×10^6 pixels per second, only every second pixel can be transferred during a scan resulting in a rate of 3×10^6 pixels per second. Even numbered pixels are transferred during one frame and odd numbered pixels during the next frame. The radar data area occupies the first 250 pixels of each raster scan line. A convenient block size in the 6/16 buffer memory is 2^{15} pixels (16K-bytes) so 128 even numbered pixels are output from each of 256 scan lines of one frame to complete one block. After the 6/16 has transferred this block from its



* See Figure 3-3 of AJJ-64.

Figure 4-5. TLI Transfer Sequence

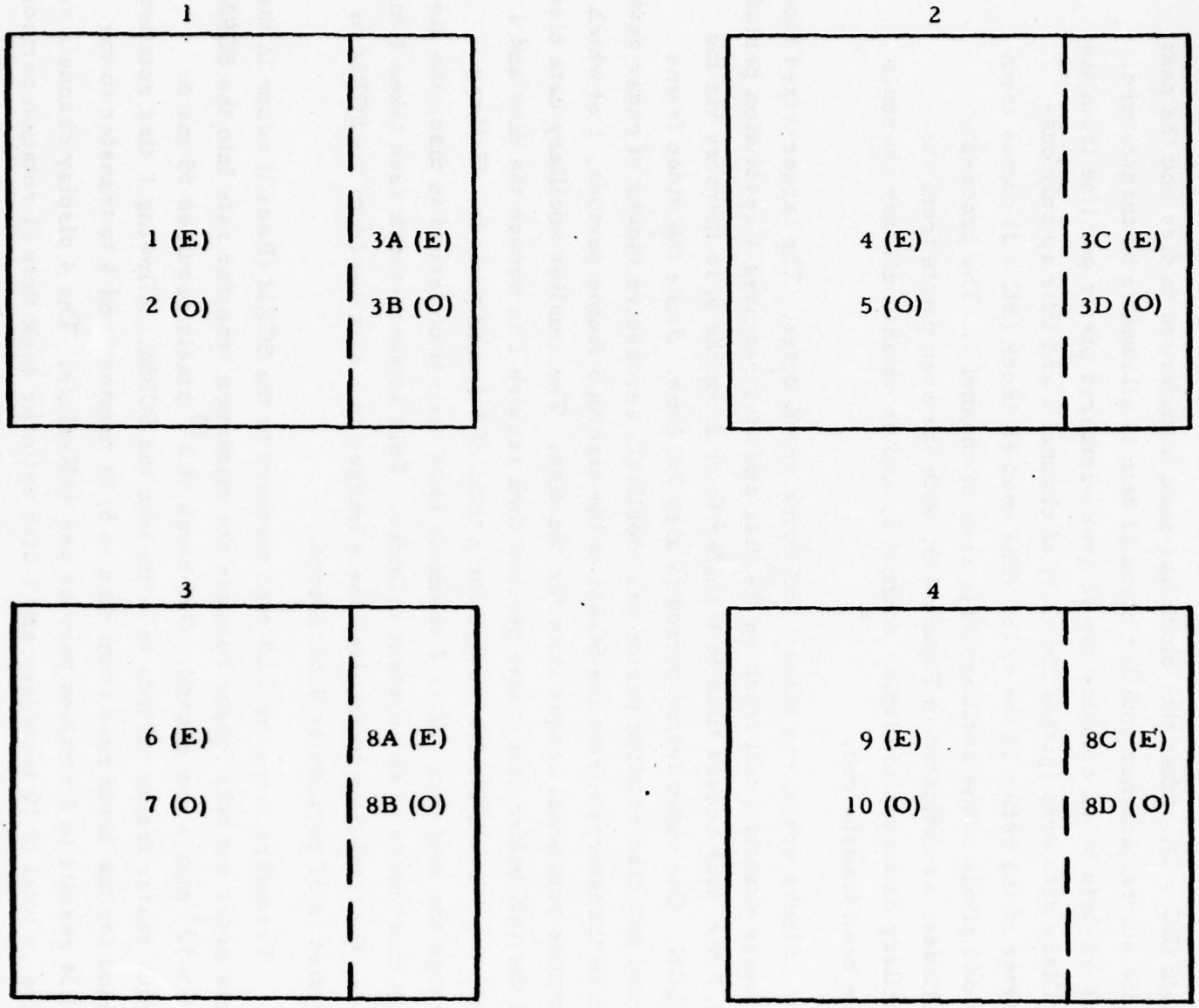
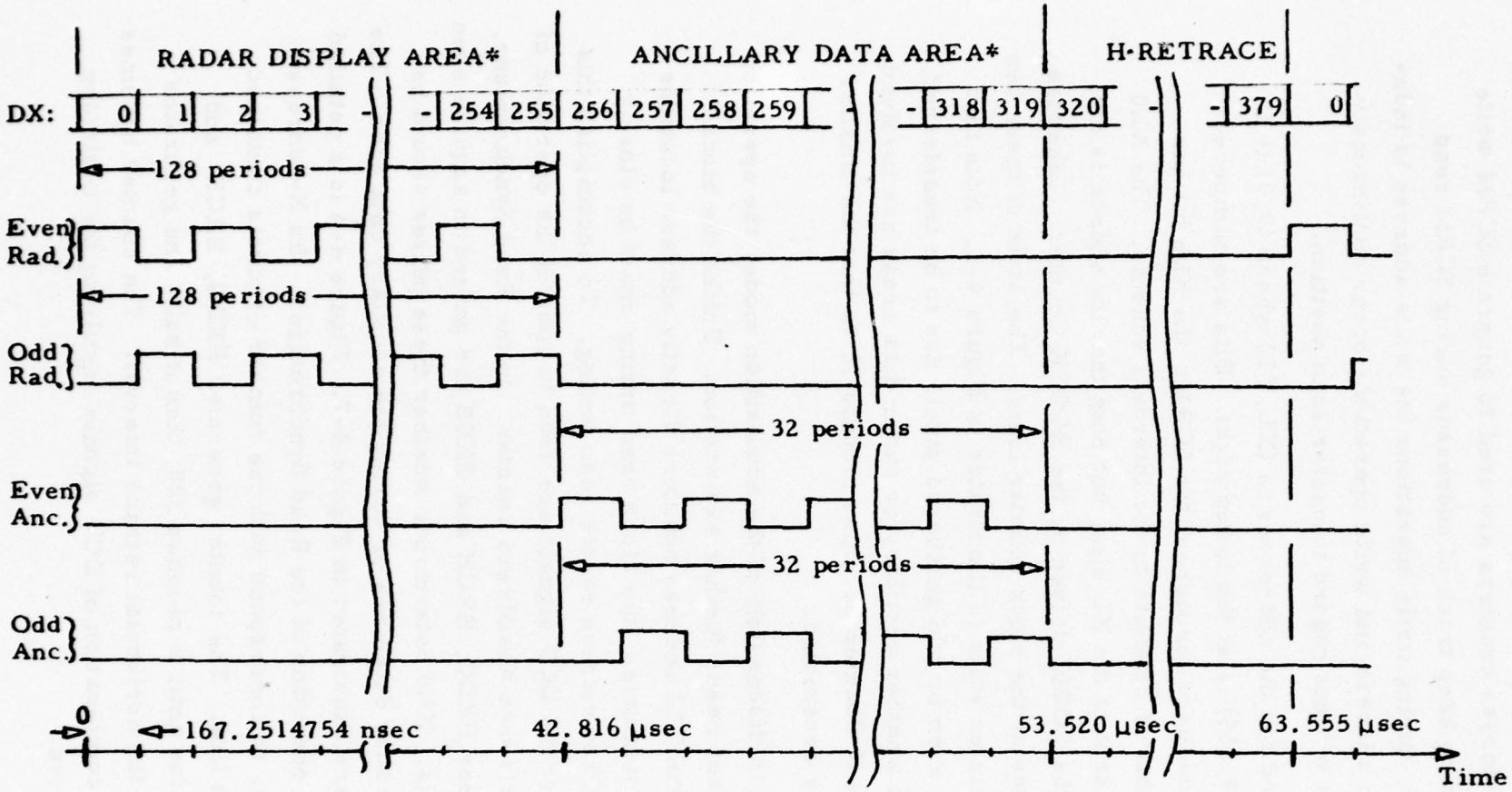


Figure 4-6. SCRM-TLS Data Transfer Order

buffer memory to the TLS disc and the next frame starts, another block of data is allowed to be transferred, this time from the odd numbered pixels (BC = 1). After this block has been transferred to disc and the next frame starts, another smaller block of data is allowed to be transferred. This 4K-byte block contains the 32 even numbered pixels per line from the ancillary data area (pixels 256-319) of channel 1 and fills up only one-quarter of the buffer in the 6/16. The next 4K block (BC = 3) comes from the odd pixels of the ancillary data area of channel 1. The process continues, as indicated in Figure 4-6, with the even points from the ancillary data area of display channel 2, and so on until all four channels have been transferred.

Blocks are of two sizes: 16K bytes or 4K bytes. The larger-sized block occupies exactly 1 full track on the disc and thus requires 1 revolution period (16.7 ms) plus access time to transfer to or from the 6/16 memory via the SELCH. One video frame period is also 16.7 ms. Since the video frame period and disc rotation period are identical, successive blocks of radar data can be transferred from the SCRM to the disc in 3 frame periods, 1 of which provides rotational access time for the disc. The smaller ancillary data blocks fill the 16K buffer in 4 frame periods then require 1 to access the disc and 1 to write the 4 small blocks on disc for a total of 6 frame periods. Halfway through the sequence, after 2 channels have been transferred to disc, the disc head must move to an adjacent cylinder. This adjacent-track seek takes 8 ms. Thus, the total time to transfer the 4 images in 1 data set from the SCRM to the disc is 37 periods or 0.62 second.

Transfers from the TLS disc memory to the SCRM (Recall) occur in the same order but take longer because the maximum transfer rate into the SCRM is 6×10^5 pixels per second. One block of 2^{15} pixels requires 55 ms or 3-plus raster frame periods to write into the SCRM. Allowing 1 disc rotation period for the block read from disc to 6/16 memory and 4 to transfer to the SCRM results in 5 rotation periods per 16K-block. The 4 display channels require a total of 10 transfers and 1 disc cylinder seek time (1 rotation period) which requires 51 disc rotation periods or 0.85 second to transfer 1 image set.



*As defined for TLS.

Note: 1) One horizontal line for each of the four possible cases is shown.
2) All lines have the same waveform within each block.
3) This waveform gates the PXDG, BRCK, and PXDS signals.
4) No waveforms are generated during either H or V retrace intervals.

Figure 4- 7. Internal READ Synchronizer Waveforms Obtained by decoding SCRM DX Scan Timing Waveforms

The same TLI address counters are used to generate SCRM write addresses as are used to keep track of addresses during SCRM read operations. However, during write operations the write address is independent of the refresh address and write operations occur continuously throughout the frames without regard to raster scan position.

The notation used for the addresses is (XL, YL) where (0, 0) is in the upper left and (319, 255) is at the lower right. Bits are numbered according to the scheme used throughout the SCRM: the XLn bit has weight 2^n--note that this is opposite to the Interdata scheme. The XL0 bit is the least significant of the XL bits, but note that its source is not the X Counter but is the LOGIC driven by the BLOCK Counter. Likewise, the MSB XL8 originates at the block counter logic. The state of these two bits for each block counter state is illustrated in Figure 4-5. Note that XL0 controls whether even or odd numbered pixels are to be transferred, while XL8 determines whether ancillary or radar data areas are involved. When XL8 is true, the X Counter becomes modulo 32 so that the smaller blocks can be properly assembled.

Returning again to discussion of the acquisition mode, the operation of the Read Synchronizer needs further explanation. Unlike the block write process where the TLI address counters directly address locations in the SCRM's image memories, the block read timing must be closely synchronized to the SCRM refresh raster scan timing. To accomplish this synchronization, numerous DCU signals are used to control the operation of the Read Synchronizer's own X-address counter. In the Read Synchronizer, XL0 determines whether PXDG, BRCK and PXDS are phased to acquire even or odd numbered pixels. XL8 determines whether these pulses should be generated during the radar data area or during the ancillary data area. The various possibilities are illustrated in Figure 4-7. Figure 4-4 is a detailed timing diagram of the operation of the Read Synchronizer. Its X-address counter is modulo 320, to correspond with the number of pixels contained within one raster scan line. The counter generates PXDG, BRCK, and PXDS throughout the line until it reaches 320; then it halts and generates no strobes throughout the horizontal retrace interval. The counter becomes active again when the combination of DCU signals signifying the beginning of a new scan line arrive.

4.3 SCRM Modifications

Previously, SCRM No. 3 was hard-wired to implement a scheme which gave highest priority, within a given display channel, to contouring and storage of radar video data. Thus, if a STORE VIDEO switch was on, no other operation (Image Transmission, DDI write, etc.) which needed access to that channel's memory bus was permitted to have it. The ACQUIRE during RECALL mode required that this scheme be altered as shown in Table 4-1.

Table 4-1. Revised SCRM Priority Scheme (within each display channel)

Priority Rank	SDF Test A or B Selected (SDFT = 1)	SDF Test A or B NOT Selected (SDFT = 0)
1	STORE VIDEO	TLS RECALL
2	SDF (TEST A or B)	STORE VIDEO
3	-	SDF (Image Transmission)
4	-	DDI (Read or Write - 7/32)

Implementation of this new scheme was done by modifying the priority logic on the MAG card so that when a given channel has been selected for recall by one of the Recall Enable command bits (see Table 4-2), all other operations are prohibited in that channel. However, the STORE VIDEO lighted pushbuttons remain on. Real time images are distinguishable from recalled images both by their order of appearance on the screen and by their time code. If either SDF test mode has been selected from the DATA TRANSMISSION CONTROL Panel, TLI and DDI operations are disabled.

Table 4-2. TLI Command and Status Bytes

	0	1	2	3	4	5	6	7
Command:	DIS	EN	ITFR	BCLR	RE1	RE2	RE3	RE4
Status:	BC0	BC1	BC2	BC3	BSY	EX	EOM	DU

6/16 Processor Device Code X'8B'

Not Used--Wired to Logic 0 for Proper SELCH Operation

There was another problem with the original configuration of the SCRM. The four MIU's each have the property of not allowing the color with code 1111 (red) to be overwritten (a solution to some range marker problems). Thus, unless the displays were erased, range and altitude markers from previous images, if located differently from those being recalled, would show through. The DDI had the same problem of not being able to overwrite red.

Since the MIU's had to be modified to solve this red overwrite problem, it was decided to also implement other additions which greatly simplify arbitration of access to various MIU busses and control lines. The implemented solution was to let the DDI have control over the RD and WD busses and the CDE and MWE control lines between the DDI and TLI while adding a new separate system for the TLI. The MIU modifications and additions which were implemented are indicated in Figure 4.9. Now, all operations of the DDI and TLI can occur simultaneously except for the case where the TLI is recalling while the DDI needs to read or write in the same channel. This conflict is arbitrated by giving priority to the TLI. The four TLI Recall Enable command bits (see Table 4-2), are or'd into the DDI's status inputs so that the 7/32 can know which display channels are available.

Changes to individual SCRM cards are summarized in Table 4-3, while affected schematics are listed in Appendix C.

Table 4-3. Modifications to SCRM Cards

Card	Description of Change	Reference
MIU (4)	• add gates to disable 1111 non-overwrite	Figure 4.9
	• add logic for PXD bus system	Figure 4.9
DDI	• or PXWE with MWE to DCU	Figure 4-2
	• run select line LASM from MAG to S257. G inputs on A1, 2, 3, 4 &7	-
MAG	• modify priority logic--add gates	Figure 4.8
	• add moultiplexer for LASM	Figure 4.8
	• add 3S drivers to enter XL, YL at Input Reg.	Figure 4.8
	• interconnect with TLI	Figure 4.2
DCU	• add butter gate for sending clock signals to TLI	Figure 4.2

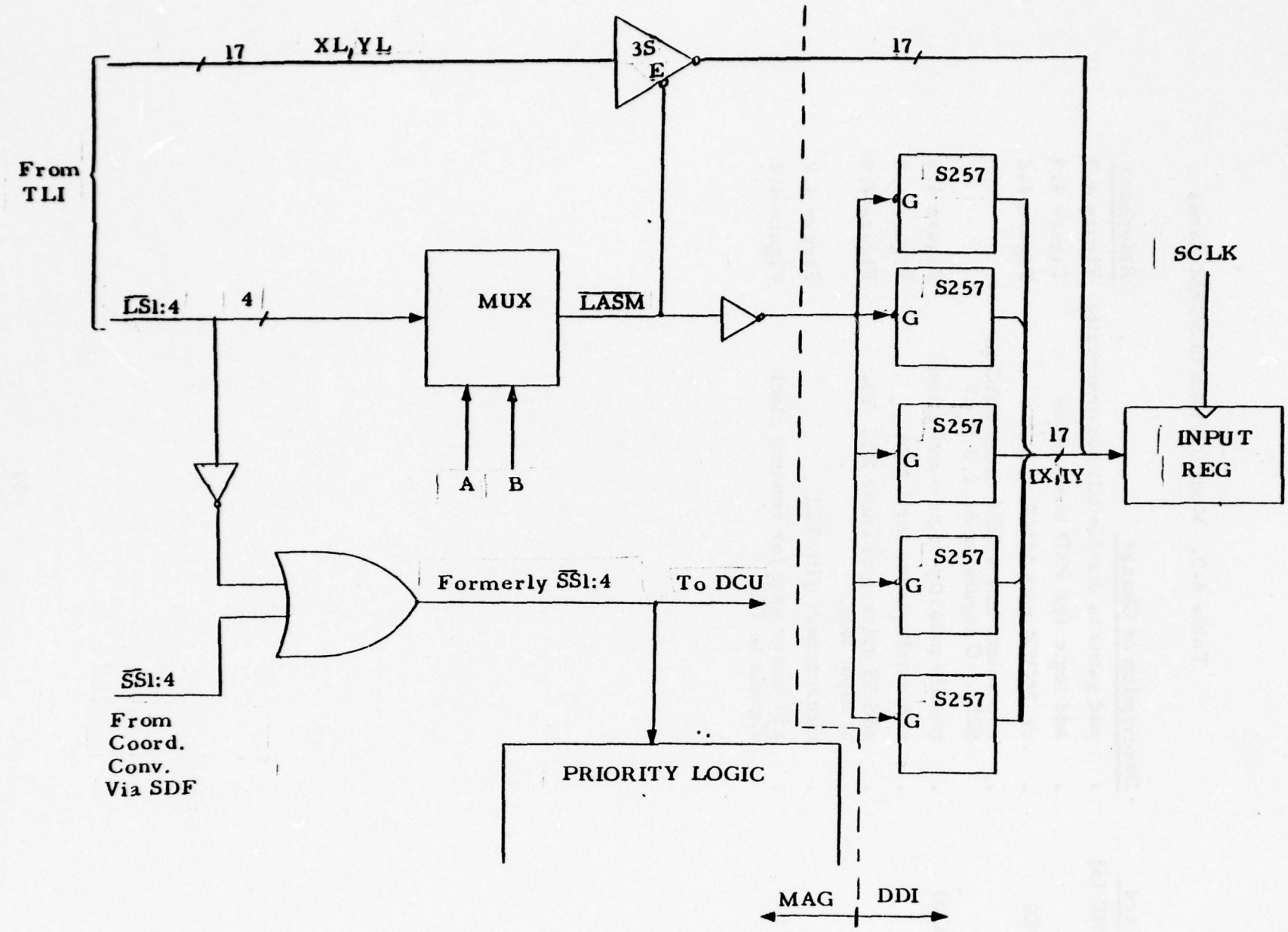


Figure 4-8 MAG Modifications

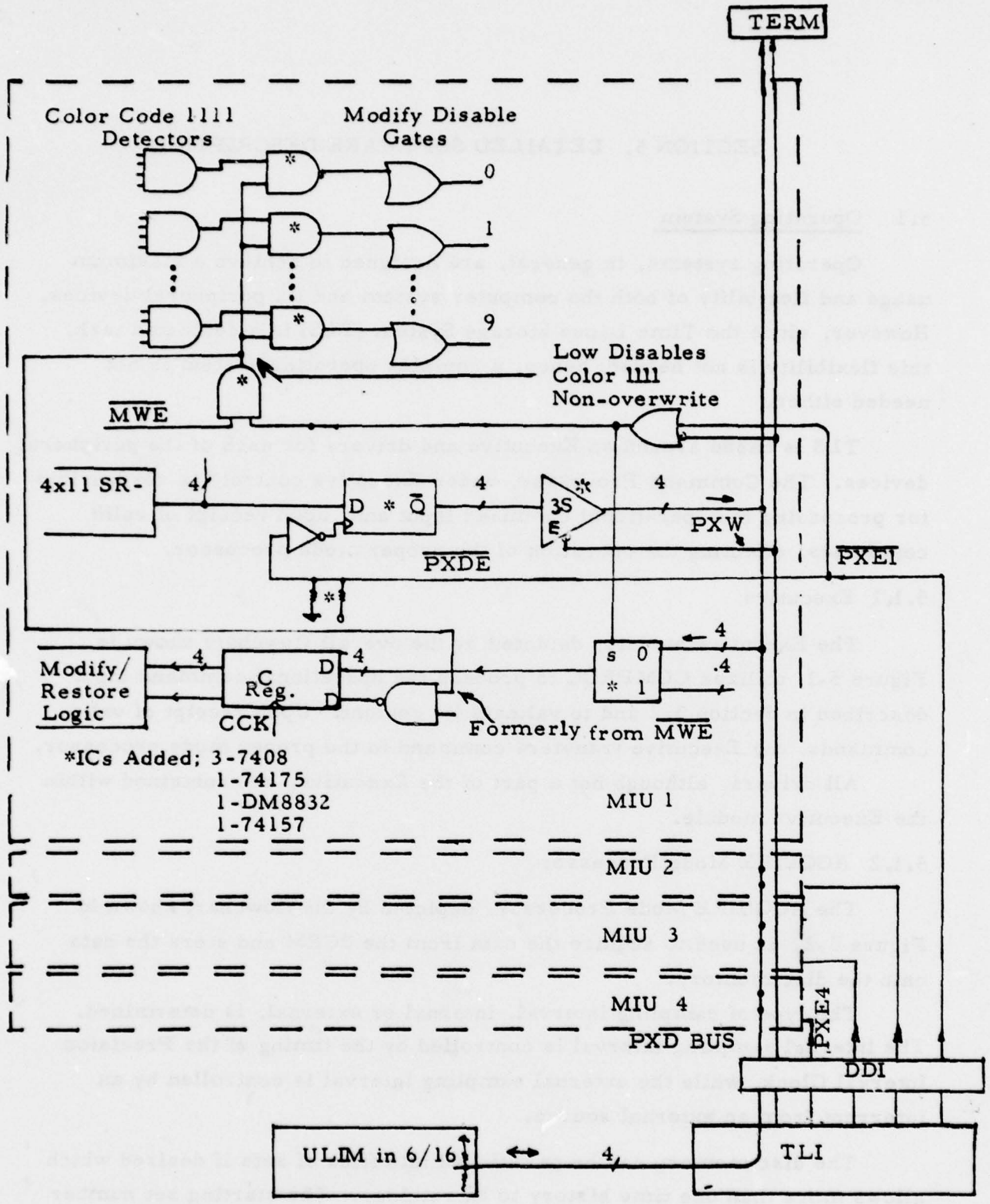


Figure 4-9. Additions to MIUs and new bus and control lines.

SECTION 5. DETAILED SOFTWARE DESCRIPTION

5.1 Operating System

Operating systems, in general, are designed to achieve a maximum usage and flexibility of both the computer system and its peripheral devices. However, since the Time Lapse Storage System (TLS) is a dedicated task, this flexibility is not needed; hence, a complex operating system is not needed either.

TLS is based around an Executive and drivers for each of the peripheral devices. The Command Processor, under Executive control, is responsible for processing the operational command input and, upon receipt of valid commands, effecting the operation of the proper mode processor.

5.1.1 Executive

The Executive module, depicted by the overall flowchart shown in Figure 5-1, utilizes COMPROC to process the operational command input described in Section 3.2 and to validate its content. Upon receipt of valid commands, the Executive transfers command to the proper mode processor.

All drivers, although not a part of the Executive, are contained within the Executive module.

5.1.2 ACQUIRE Mode Processor

The ACQUIRE Mode Processor, depicted by the flowchart shown in Figure 5-2, is used to acquire the data from the SCRM and store the data onto the disc memory.

The type of sampling interval, internal or external, is determined. The internal sampling interval is controlled by the timing of the Precision Interval Clock, while the external sampling interval is controlled by an interrupt from an external source.

The disc memory can be partitioned into files of sets if desired which allows more than one time history to be retained. The starting set number of the file and the number of sets in the file are extracted from the command message and the general housekeeping is set up.

The Acquire processor then sets the Acquire timer for the specified acquisition interval and returns control to the Executive until this time interval has elapsed. At that time the acquire timer is set again if more sets are to be acquired, and the radar data portion of the selected display channels is obliterated to clear any range markers resulting from prior recall sequences. Also, the delay timer is set for the delay time requested, recall is inhibited, and control is again returned to the Executive until the delay interval has elapsed. At that time subroutine Getset (Figure 5.3) acquires data from the displays and transfers it onto the disc memory in blocks of 16,384 bytes until all data for the four displays have been recorded.

After all requested sets for this file have been acquired, a test is made to determine if cyclical output has been requested. Cyclical output is defined as continuing the acquisition process after all requested sets have been recorded by starting the output recording at the beginning of the current file.

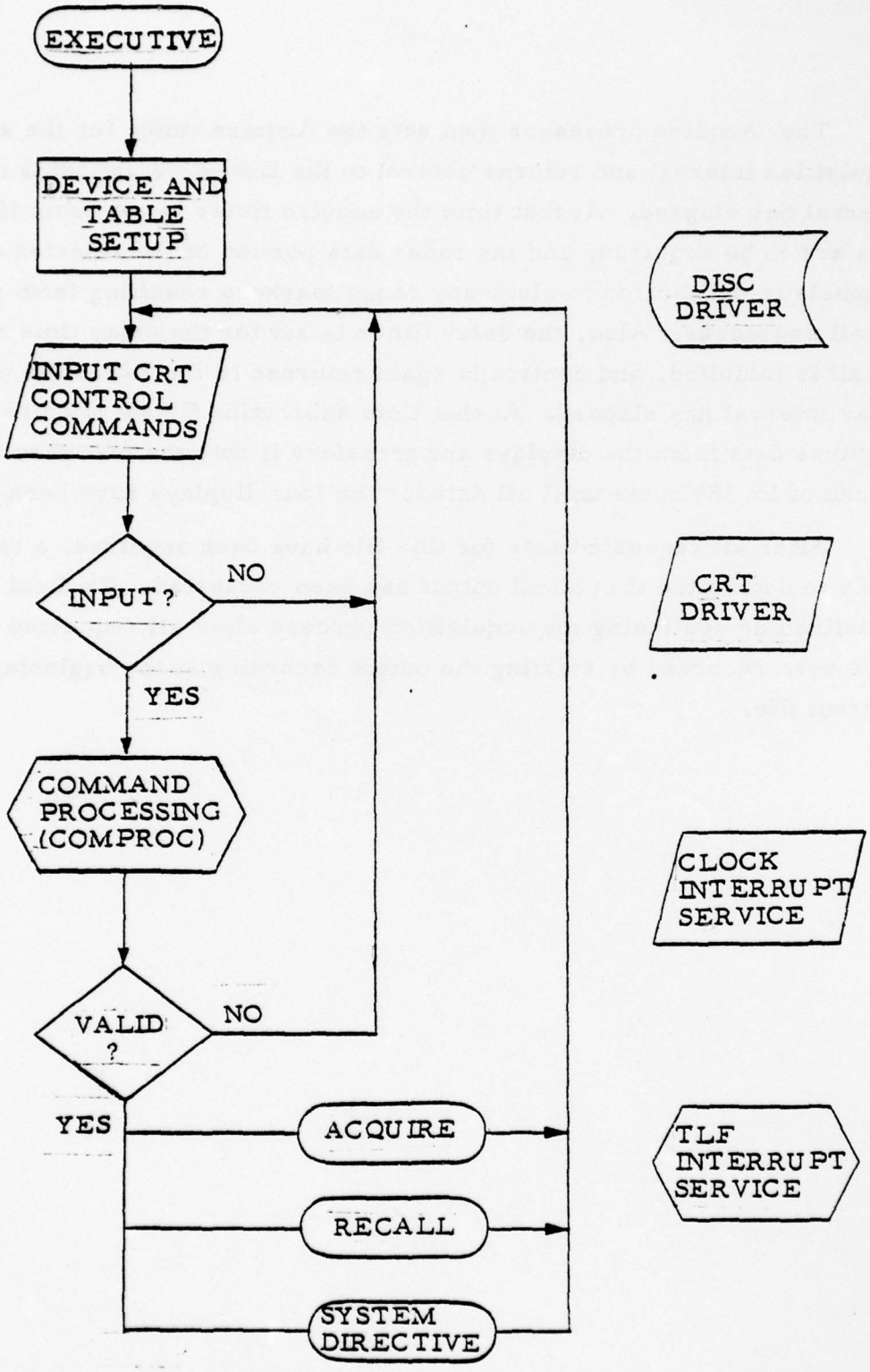


Figure 5-1 Executive Flowchart

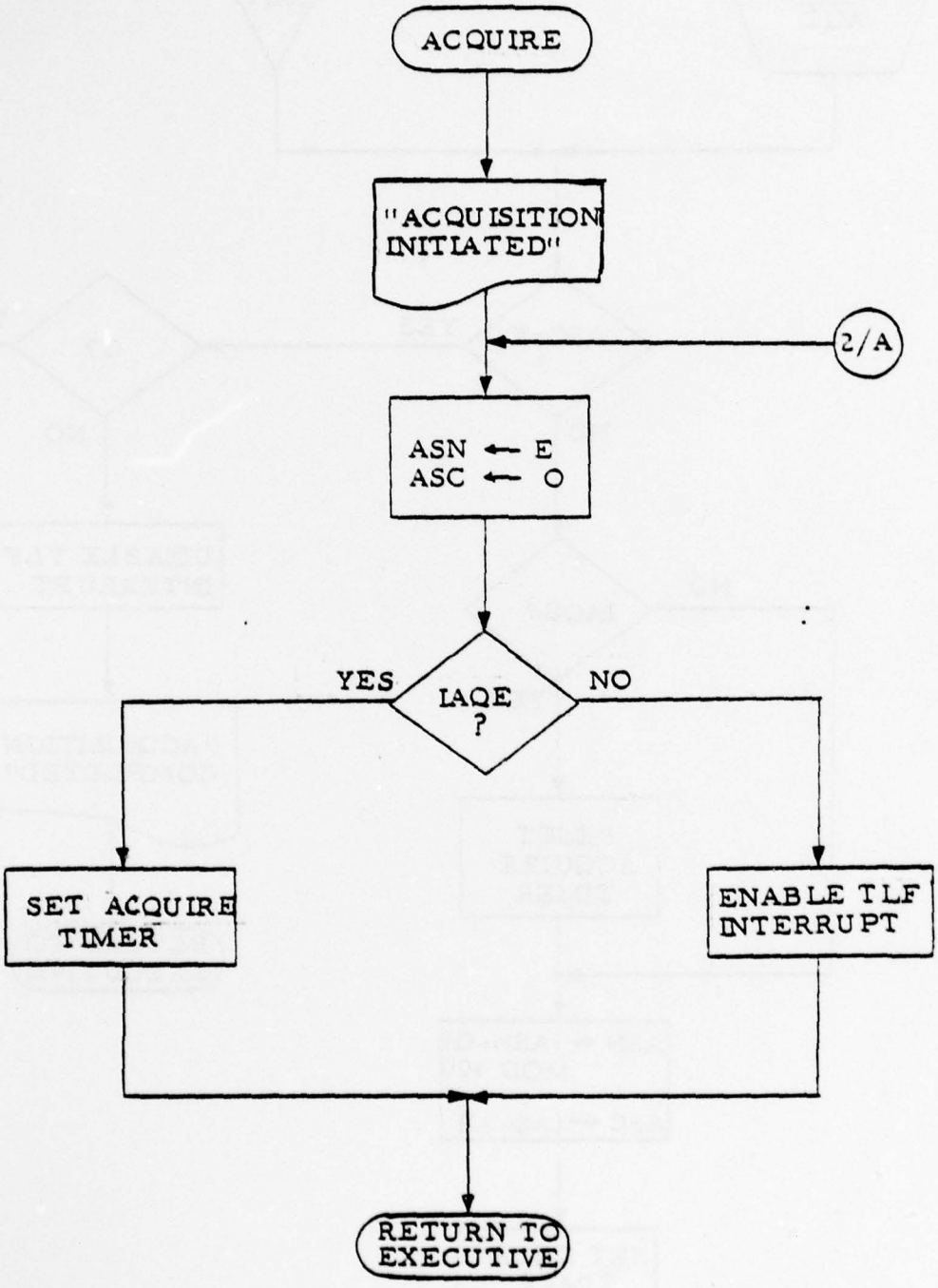


Figure 5-2 ACQUIRE Mode Processor (Page 1 of 3)

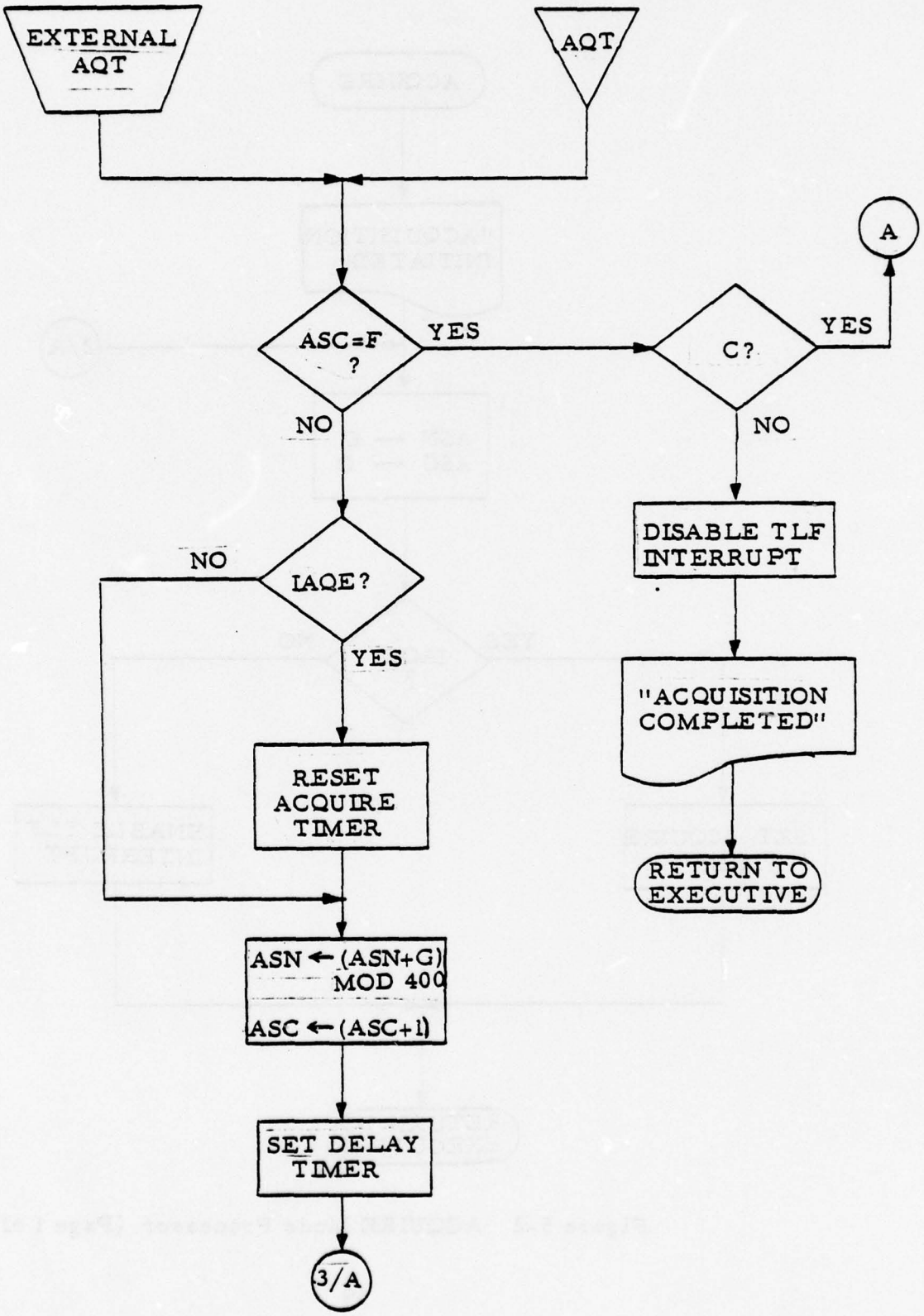


Figure 5-2 ACQUIRE Mode Processor (Page 2 of 3)

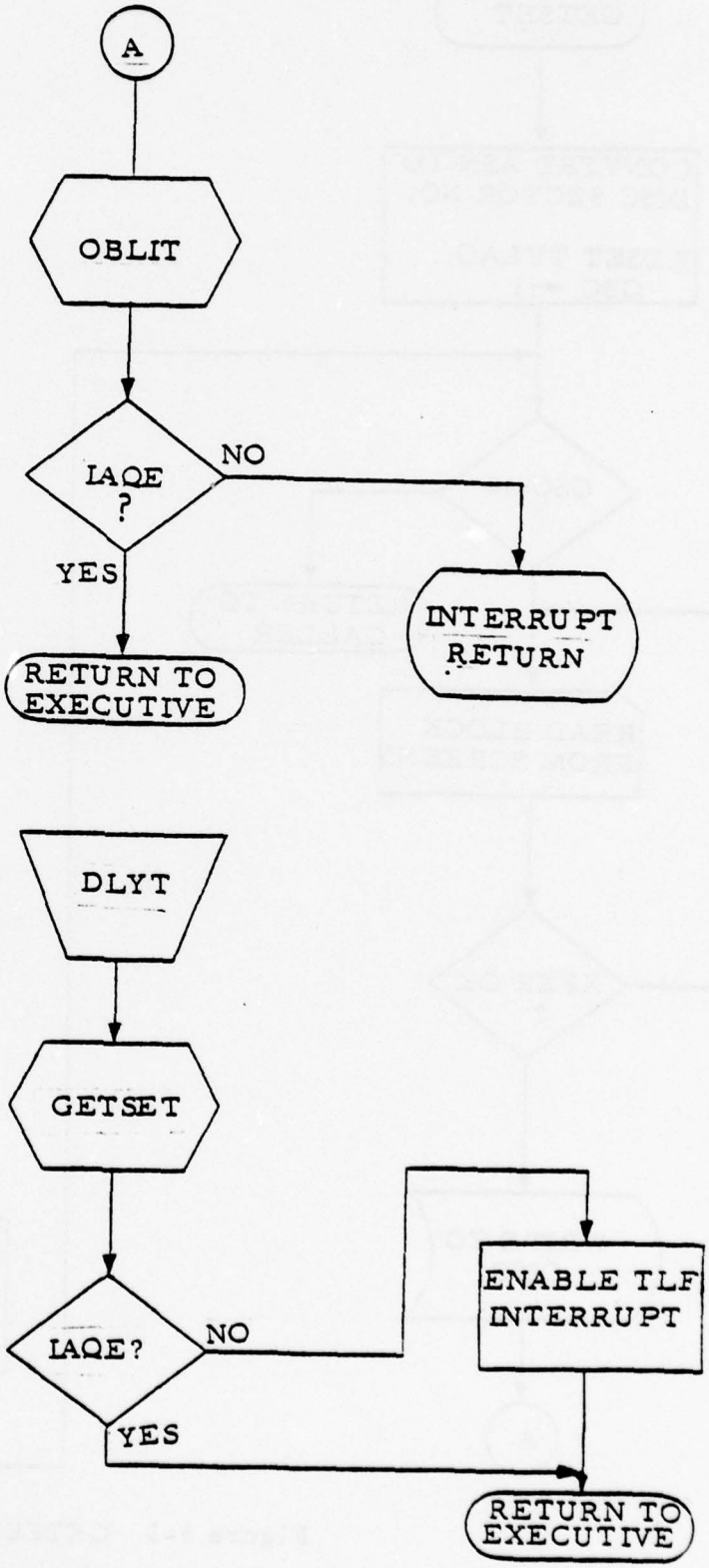


Figure 5-2 ACQUIRE Mode Processor (Page 3 of 3)

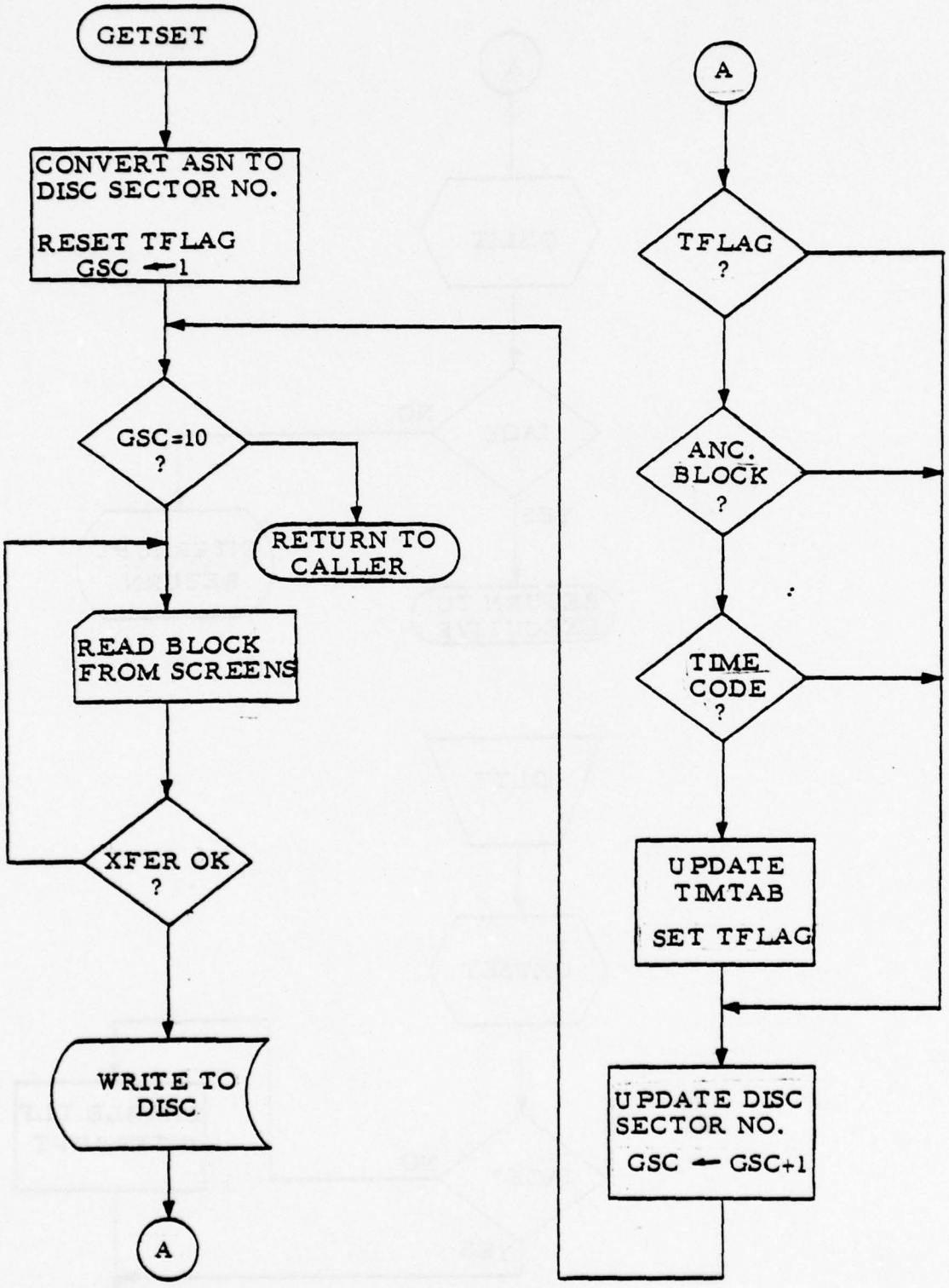


Figure 5-3 GETSET Flowchart

5.1.3 RECALL Mode Processor

The RECALL Mode Processor, depicted by the flowchart shown in Figure 5-4, is used to recall the previously acquired data block from the disc memory and output it to the SCRM for display on the available display channels.

The display channel(s) to be accessed by the TLS recall process are selected. The remaining channels become available to another system and the TLI will be commanded to bypass the output of data to them.

The mode of RECALL, manual or automatic, is then extracted from the command message and is used to control the display of the time history data.

5.1.3.1 Manual Recall

The set number increment or decrement is extracted from the command and added algebraically to the current recall set pointer. The requested data are input from the disc memory and output to the TLI driver in blocks of 16,384 bytes until one entire set has been transferred. The recall mode processor then relinquishes control back to the Executive.

5.1.3.2 Automatic Recall

The starting set type, either by time of acquisition or set number and number of sets to recall are extracted and used to determine the parameters for the disc addressing. The starting set number is extracted for the set number type; the starting time is extracted for the time type. The starting set for the time type is defined as the set with time code numerically closest, within sixty minutes, of the specified time. A set increment, which is used to allow bypassing the next N-1 sets, is also extracted from the command; no bypass will take place if the increment field is left blank. Finally, the display interval (time between sets) is extracted from the command and the interval timer is forced to this value to start the processing cycle.

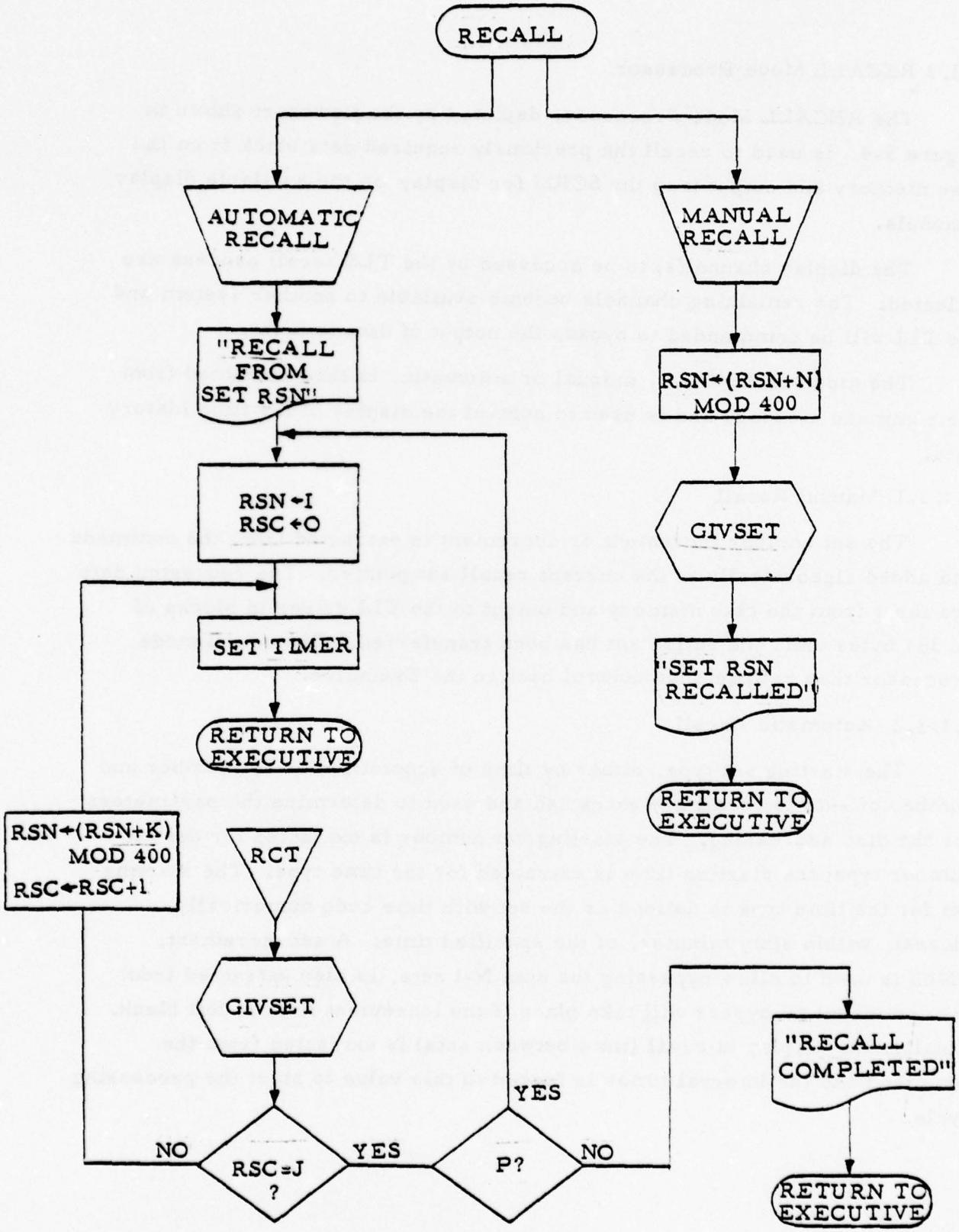


Figure 5-4 RECALL Mode Processor

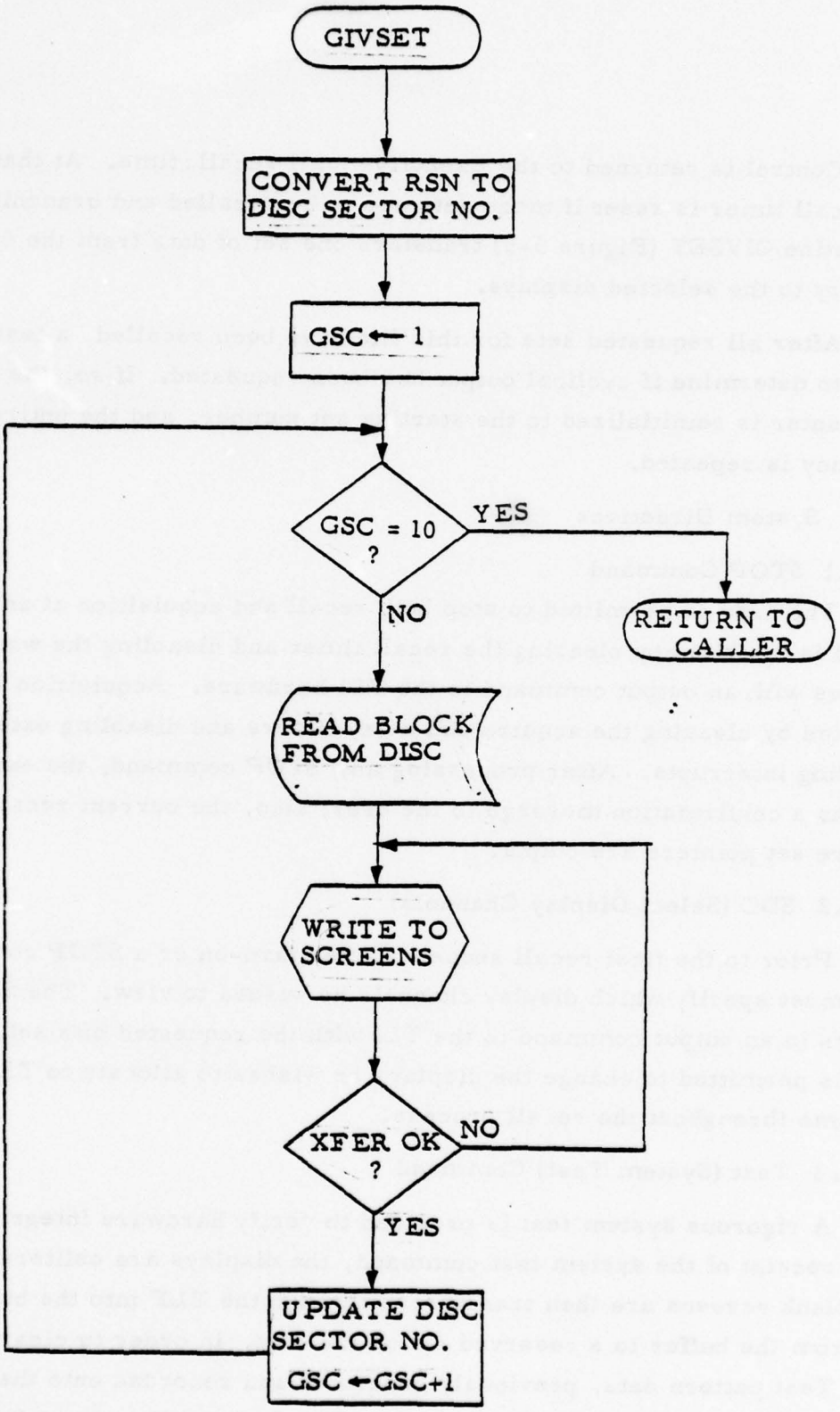


Figure 5-5 GIVSET Flowchart

Control is returned to the Executive until recall time. At that time the recall timer is reset if more sets are to be recalled and branching to subroutine GIVSET (Figure 5-5) transfers one set of data from the disc memory to the selected displays.

After all requested sets for this file have been recalled, a test is made to determine if cyclical output has been requested. If so, the recall set counter is reinitialized to the starting set number, and the entire recall sequency is repeated.

5.1.4 System Directives

5.1.4.1 STOP Command

The user is permitted to stop both recall and acquisition at any time. Recall is inhibited by clearing the recall timer and disabling the write process with an output command to the TLI hardware. Acquisition is inhibited by clearing the acquire and delay timers and disabling external sampling interrupts. After processing any STOP command, the executive returns a confirmation message to the user; also, the current recall and acquire set pointers are output.

5.1.4.2 SDC (Select Display Channels)

Prior to the first recall sequence after turn-on or a STOP command, the user must specify which display channels he wishes to view. The SDC command results in an output command to the TLI with the requested bits set. The user is permitted to change the displays he wishes to allocate to TLS at any time throughout the recall process.

5.1.4.3 Test (System Test) Command

A rigorous system test is provided to verify hardware integrity. Upon receipt of the system test command, the displays are obliterated. The blank screens are then transferred through the TLF into the buffer and from the buffer to a reserved set on the disc, in order to clear that set. Test pattern data, previously generated and recorded onto the disc, are retrieved and output to all displays. The data are then input from the displays and output to the cleared, reserved set on the disc. After the screens are blanked these data are then transferred to the displays, and, hopefully, the user will find them identical to the prerecorded patterns he viewed initially.

5.2 Drivers

The drivers, wherever possible, were patterned after the existing Interdata drivers for compatibility. Mnemonics, entry point names, and returned status bits are some of the areas in which this effort was concentrated.

5.2.1 Disc

The disc is a high-speed random-access magnetic storage device upon which data are stored in individually addressable sectors, each of which holds 256 8-bit bytes. A record must begin at the first byte of any sector, and may be of any length (up to memory size limitations) since the disc hardware automatically sequences to the next sector when the current sector has been transmitted.

The disc driver was written to be able to handle both the 10 MB and the 80 MB disc systems. Since the 10 MB disc is comprised of a 5 MB fixed and a 5 MB removable cartridge which share one seek mechanism, they were considered separate devices.

5.2.1.1 Supported Attributes

Read, Write, Wait, Unconditional Proceed
Read Check
Variable Length Records

5.2.1.2 Functional Description

Read: Data are read from the disc starting at the specified sector into the user buffer until the buffer is full. If an attempt is made to read beyond the end of the disc, end of medium status is returned.

Write: Data are written from the user buffer to the disc, starting at the specified sector, until the buffer is empty. Attempts to write past the end of the disc cause end of medium status to be returned. In this case, no data is transferred.

Errors on data transfers cause the operation to be retried five times before returning error status.

Read Check: A read check operation is performed on the sector specified.

All data transfers start on a sector boundary but may end on any byte of a sector.

5.2.1.3 Status Definition

Status	Meaning
X'00'	Normal completion.
X'A0'	Request could not be started, device not ready.
X'90'	End of medium. Transfer ends beyond the end of the disc.
X'88'	Pseudo end of file mark read. This status is only returned on request.
X'84'	Seek incomplete. All device errors other than data transfer error.
X'82'	Data transfer error after five retries. Write protect violation. Timeout.
X'81'	Defective Track from Read Check.

5.2.2 Clock

The Universal Clock Module provides a precision interval clock as well as a line frequency clock to generate processor interrupts under program control.

The precision interval clock is derived from a crystal-controlled oscillator permitting program selection of clock frequencies of 1 kHz, 10 kHz, 100 kHz, or 1 MHz as well as count intervals from zero to 4095. Interrupts can be generated at time intervals from one microsecond to 4.095 seconds.

The line frequency clock, which has a separate device address from the precision clock, derives its clock source from the AC power line. When enabled under program control, the line frequency clock generates interrupts at a 120 Hz rate.

The two clock functions are assigned consecutive even/odd device addresses and may be operated independently or simultaneously if desired.

5.2.2.1 Functional Description

The time-out constant is established by the driver initiation routines. It is used to time events such as SELCH hang-up, loss of data transfer, etc. The value of the timeout constant is defined as follows:

- -1 (X'FFFF') means the I/O request is in the process of normal termination by the driver.
- 0 (X'0000') means the driver should abnormally terminate the I/O request.
- 2^{15}-1 (X'7FFF') means the I/O request is not to be timed out by a timer interrupt.
- 1 through X'7FFE' means the timeout constant is to be decremented by 1 every second by the system clock until the value is zero.

5.2.3 PASLA

The Programmable Asynchronous Single Line Adapter (PASLA) provides an interface between the multiplexer I/O bus and any asynchronous data set or local terminal with an RS-232C interface.

All data transfers between the PASLA and data set and control lines generated and monitored to/from the data set are under program control by providing proper status and interrupt information to the processor. Additionally, line attributes such as baud rate (one of two pre-selected rates), character length (5, 6, 7 or 8 bits), parity (odd, even, or none), and number of stop bits (one or two) are also under program control.

Communications through the interface can be either full-duplex or half-duplex and conform to RS-232C specifications. Switch selectable baud rates are 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19.2K.

Data are transferred between the PASLA and the modem or terminal bit-serial at the selected baud rate. The PASLA module includes circuits to detect and generate signals that set-up, take-down, and supervise the communications channel, and provide status and interrupt information to the processor.

5.2.3.1 Supported Attributes

Read, Write, Wait, Unconditional Proceed, Image Variable

5.2.3.2 Functional Description

Read ASCII: Data read are masked to 7-bit ASCII. Data are read until the buffer is full, or a carriage return is found, whichever occurs first. Upon termination, a carriage return-line feed sequence is sent to the printer.

Write ASCII: The buffer is scanned to eliminate trailing blanks. Data are then output until the buffer is exhausted and a carriage return-line feed sequence is output.

Read or Write Image: None of the above formatting actions occur. The amount of data requested is typed out or read in, without masking to 7-bit ASCII.

5.2.3.3 Status Definition

Status	Meaning
X'00'	Normal completion
X'82'	Time out or Break
X'84'	I/O Error
X'A0'	Device Unavailable

5.2.3.4 Notes

Strapping Options: The PASLA must be strapped for Full Duplex (FDX) operation, Disable CARR Status, Disable DSRDY Status, Disable CL2S Status.

5.2.4 TLF

The Time Lapse Formatter (TLF), mounted on the Universal Logic Interface Module (ULI), provides an interface between the SELCH bus and the Time Lapse Interface (TLI).

All data transfers between the TLF and the TLI are under program control by providing proper status information to the processor. The data are transferred between the memory and TLF via the SELCH bus.

5.2.4.1 Functional Description

Read: Data are read from the TLF into the user buffer until the buffer is full.

Write: Data are written from the user buffer to the TLF until the buffer is empty.

Errors on data transfers cause the operation to be repeated.

5.3 System Expansion

By design, this operating system does not make optimum use of its resources. If desired, however, the user can expand the system to meet whatever needs may arise. For instance, the ability to write out the BCD time table to the CRT might be of great use.

Also, providing the capability of writing a certain display of a stored set to a different display has been suggested. All these types of operations can be done, but they would involve significant program development on the 7/32 processor. Facilities are provided to load programs from the 7/32 to the 6/16 and these are described in Appendix B.

APPENDIX A

TIME LAPSE FORMATTER DIAGNOSTIC TEST

A diagnostic test feature is provided to test the Time Lapse Formatter (TLF) portion of the TLS hardware. This program, TLFTEST is a modified version of the standard Interdata Universal Logic Interface Test. TLFTEST is included with the TLS system's program listings and contains a full explanation of the test and the errors it will discover. To run TLFTEST, it must first be loaded from the 7/32 to the 6/16 as described in Appendix B, with Step 5 being: ASl, TLFTEST.OBJ. Next, the jumper connections described in the program listing must be made. Finally, depress DTA, 4000, ADDR, INI, and RUN. If no errors are found, the malfunction is probably within the TLI and cannot be traced with software techniques.

APPENDIX B

DISC DIRECTORIES AND SOFTWARE DEVELOPMENT AIDS

A portion of the MSM-80 Disc has been reserved for the purpose of saving the TLS system programs, diagnostic programs, software development aids for communication with the 7/32 Processor, or user-created programs.

The procedure for transferring a disc file to the 6/16 core was described in Section 3.1.1 for the case of TLS system programs. When the user desires a different file, the only step that must be altered is to enter in a different directory number to location X'7E'. The following table summarizes the contents of the disc files:

Location X'7E'	Start Location of Program	Program
X'0111'	X'0400'	TLS System
X'0222'	X'4000'	Dump Core to Disc File
	X'6000'	Load from 7/32 to 6/16
X'0333'	Not Reserved	
⋮		
X'0999'		

The user may desire to run his own programs on the 6/16 Processor. To achieve this, he must first have error-free assembled program(s) on file within the 7/32 Processor. The remainder of the procedure is as follows:

1) Transfer MSM-80 Disc file X'0222' to the 6/16.

2) Slide the PASLA (slot number 4) out. Locate the DIP switch, upon which switch 2 is labeled DSR. Move this switch to the ON position. Slide PASLA back in.

3) Connect a cable between the 7/32 Processor's PASLA (Slot number 5) and the 6/16's PASLA

4) On the 7/32 Carousel, enter:
```
T  .BG
L  .BG, M17OUT
O   R
AS2, LIPC:
```

5) On 7/32 Carousel, enter: AS1, PROGNAME

6) On 6/16 Console, depress: DTA, 6C08, ADDR, INI, RUN.

7) On 7/32 Carousel, enter: ST.

If the user desires to load and link two or more programs, he should return to Step 5 and proceed as before; however, 6 now is merely:

6) Depress RUN.

After all programs have been loaded enter O NON on the 7/32 carousel. Also, reset the PASLA's DSR switch and remove the PASLA connector cable.

The user may determine that his programs are useful enough to be stored on the MSM-80 disc for future use. This facility is provided; however, it is to be used with utmost care.

The user should never store his programs into files 1 or 2, as they are reserved. The procedure is as follows:

1) Transfer MSM-80 disc file X'0222' to the 6/16.

2) Load programs from 7/32 Processor as outlined previously.

3) On 6/16 console, depress: DTA, 4000, ADDR, INI, RUN.

4) The processor should halt.

5) Depress DTA, a file number, q, between 3 and 9, and RUN.

The contents of core are now stored on the disc with a directory number X'0qqq'.

APPENDIX C

LIST OF SCHEMATICS

The following are new schematics:

Description	Drawing #
MAG/TLI (Sheet 2)	SD914333
TLF	SD998432
Cable Diagram - TLF to MAG/TLI	SD998433
Cable Diagram - MAG/TLI to DCU and DDI	SD998434

The following SCRM3 schematics were modified:

MAG/TLI (Sheet 1)	SD914333
DDI	SD913323
DCU	SD913324
MIU	SD914334
SCRM3 Master	SD914329

APPENDIX D

PRODUCT INFORMATION BULLETINS

INTERDATA

PERIPHERALS

MSM80

Removable Media Mass Storage Module

PRODUCT DESCRIPTION

Interdata's MSM80 Removable Media Mass Storage Module is a large capacity, high performance disc storage subsystem for use with Interdata's 16- and 32-bit computer systems. The basic subsystem provides a formatted 67.2 million bytes of storage with expansion capability to over 268 million bytes by the addition of three MSM80E modules.

The MSM80 basic subsystem provides the user with a disc storage drive, fully formatted 67.2 million byte disc pack and a controller capable of handling four storage drives. The MSM80E consists of a disc storage drive and fully formatted 67.2 million byte disc pack.

FEATURES

- 67.2 million byte formatted capacity
- 1.2 million bytes/second transfer rate
- 3330 – type technology
- 30 ms average seek time
- 8.3 ms average rotational latency time
- Fast start-up
- Pack interlock
- Write protect

OPERATIONAL CHARACTERISTICS

Both the MSM80 and MSM80E contain 3330-type technology storage drives utilizing 5 platter removable disc packs. Access time ranges from 7 ms for a track-to-track seek to a 55 ms for a maximum track seek. On the average, only 30 ms is required to position the heads. The rotation speed is 3600 RPM resulting in an average rotational latency of only 8.3 ms. The data transfer rate is a very high 1.2 million bytes per second.

A highly accurate closed loop proportional servo system is employed to assure extremely rapid and precise head positioning by providing a feedback loop to the voice coil head actuator mechanism. The servo system uses one recording surface as a servo reference which contains timing marks. Only three of the five platters are actually used as recording surfaces.

Data security is assured by providing a write protect feature with positive manual control, electronically inhibiting write functions upon detection of seek errors, track position error, loss of rotational speed or loss of voltage. Pack damage is prevented by a positive pack interlock mechanism. As further assurance, the heads are retracted when a voltage or rotational speed loss error condition occurs.

Dual Port options are available for both the MSM80 and 80E. This option allows two processors to share a single MSM subsystem on an exclusive access basis. Sophisticated detection circuitry is self-contained to provide automatic deselection when power fail, open cable or internal program failure conditions occur.

The MSM80 is supported by Interdata 16- and 32-bit computer standard operating systems with data transfer via the direct memory access port using a Selector Channel. Complete data recovery facilities are included which invoke data strobe offset and track offset sequences for read recovery in the event of read errors. Software support is confined to single port MSM subsystems.

SPECIFICATIONS

Capacity

Bit Density	6000 bits per inch (2.54 cm) nominal
Track Density	384 tracks per inch (2.54 cm)
Cylinders	823
Tracks per Cylinder	5
Bytes per Sector	256
Sectors per Track	64
Formatted	67,200,000 bytes

Access Times

Average Access Time	30 milliseconds
Average Rotational Latency	8.3 milliseconds
Average Start Time	25 seconds
Average Stop Time	20 seconds

Dimensions

Storage Module	
Height	34 inches (86.4 cm)
Width	19 inches (48.3 cm)
Depth	34 inches (86.4 cm)
Weight	243 pounds (110 Kg)
Controller	15 x 15 (38.1 x 38.1 cm) inch printed circuit boards, 2 required

Power

Storage Module	120 VAC, 8.2 Amperes (max), 60 Hz, Single Phase, Starting Current 30 Amperes 220 VAC, 4.9 Amperes (max), 50 Hz, Single Phase, Starting Current 22 Amperes
Controller	+5 VDC, 7 Amperes

Environmental

Temperature	59 to 90° F (15 to 32.2° C) operating
Humidity	20 to 80% Relative Humidity (no condensation)

INTERDATA PRODUCT NUMBERS

M46-600 Model MSM80, 67,000,000 Byte Removable Media Mass Storage Module, Drive and 1 x 4 Controller. This unit is a 3330-type disc drive using a 5-surface disc pack. Disc transfer rate is 1,200,000 bytes per second, average access time is 30 ms. Storage capacity is 67,200,000 bytes fully formatted. Includes a fully formatted disc pack, write protect feature, damage preventing pack interlock, pedestal cabinet and controller capable of handling up to four disc drives. 60 Hz.

M46-601 Model MSM80E, 67,000,000 Byte Removable Media Mass Storage Module, Expansion Drive. This unit is a 3330-type disc drive using a 5-surface disc pack. Disc transfer rate is 1,200,000 bytes per second, average access time is 30 ms. Storage capacity is 67,200,000 bytes fully formatted. Includes a fully formatted disc pack, write protect feature, damage preventing pack interlock and pedestal cabinet. 60 Hz.

M46-602 Same as M46-600. 50 Hz.

M46-603 Same as M46-601. 50 Hz.

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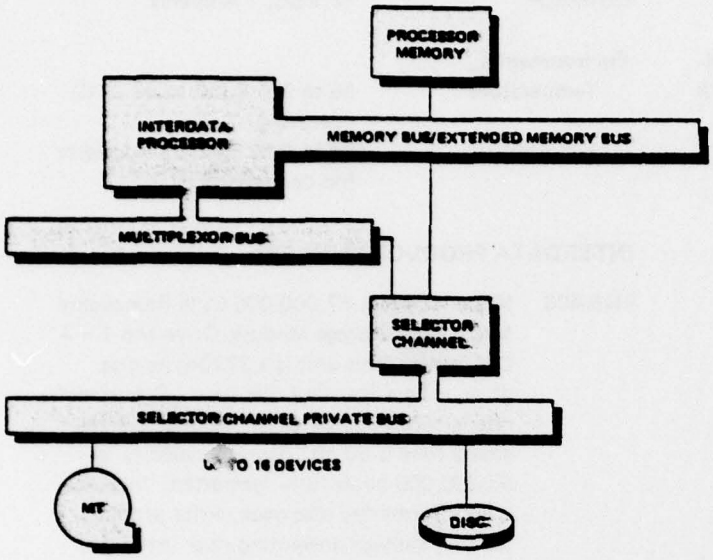

Selector Channel

PRODUCT DESCRIPTION

The Selector Channel provides a completely independent high-speed direct memory data transfer interface between Interdata processor memory and selected device controllers. Up to 16 device controllers can be connected to the Selector Channel.

Data transfer rates of up to 2,000,000 bytes per second are possible. The Selector Channel provides the capability to transfer data simultaneously with data transfer over the multiplexor bus and other processing functions.

The Selector Channel can operate in a block-transfer mode or a transparent mode and allows device data transfer in a byte or halfword data format.

FEATURES

- 2,000,000 Bytes Per Second Transfer Rate
- Simultaneous Data Processing
- Byte and Halfword Data Transfer Modes
- True Cycle Stealing Direct Memory Access

OPERATIONAL CHARACTERISTICS

The Selector Channel transfers data by employing a true cycle-stealing operation directly to processor memory. Once initiated, the Selector Channel functions in a completely autonomous fashion. One device can be active at any one time.

Data transfer is initiated by loading a starting address and an ending address which specify the memory start and end addresses for the specific data to be transferred. After address loading, the processor issues a GO command to the Selector Channel and the data transfer proceeds without further direction from, or interaction with the processor. The GO command also inhibits activity between the processor and any other device on the Selector Channel private bus. All Selector Channel set-up commands are transferred over the processor multiplexor bus.

The M70-103 Selector Channel is designed to function with Interdata 16-bit processors with a memory address range of 64 K bytes. The M73-105 Extended Selector Channel is used with the 7/32 series processors and is capable of addressing 1 million bytes of memory.

COMMANDS

The Selector Channel responds to three commands: READ, GO and STOP.

The READ command causes the Selector Channel to set the particular device controller in a read mode and the internal memory interface logic to a memory write mode. This allows data to transfer from the Selector Channel connected device to memory. In the absence of a READ command, the Selector Channel automatically assumes a WRITE mode which sets the memory interface logic to transfer data from memory to a Selector Channel connected device.

The GO command releases the internal Selector Channel circuitry which allows the direct memory access operations to take place and the autonomous transfer of data to proceed until the block specified by the start and end addresses has been completed.

On receipt of a STOP command, the Selector Channel completes the current access cycle, clears the busy signal which will allow the processor access, and terminates direct memory access operations.

On termination of a data transfer block, the Selector Channel may interrupt the processor to signal activity completion or change the status to return the Selector Channel to idle mode without processor interrupt.

When not activated, the Selector Channel private bus is connected directly to the multiplexor bus and acts as a bus buffer. Communication between the multiplexor and private bus devices takes place in the normal I/O bus manner using standard I/O programming conventions.

SPECIFICATIONS

Maximum I/O Data Rate:
2,000,000 bytes per second

Maximum Number of Devices:
16

Data Transfer Format:
Byte (8 bit) or Halfword (16 bit)

Direct Memory Access Method:
Cycle Steal

Address Range:

Selector Channel	64 K Bytes
Extended Selector Channel	1 M Bytes

Dimensions:
15" x 15"

Weight:
2.5 pounds

Power Requirement:
+ 5.0 VDC ± 5%, 2.5 Amperes

Interdata Product Number

M70-103 – Selector Channel. Provides true cycle-stealing to memory for 8 or 16-bit transfers at rates up to 2MB/sec. Includes hardware byte/halfword assembly and automatic control of variable length records.

M73-105 – Extended Memory Selector Channel. Provides a true cycle stealing access to up to 1,000,000 bytes of main memory for 8 or 16 bit transfers at rates up to 2 MB/sec.

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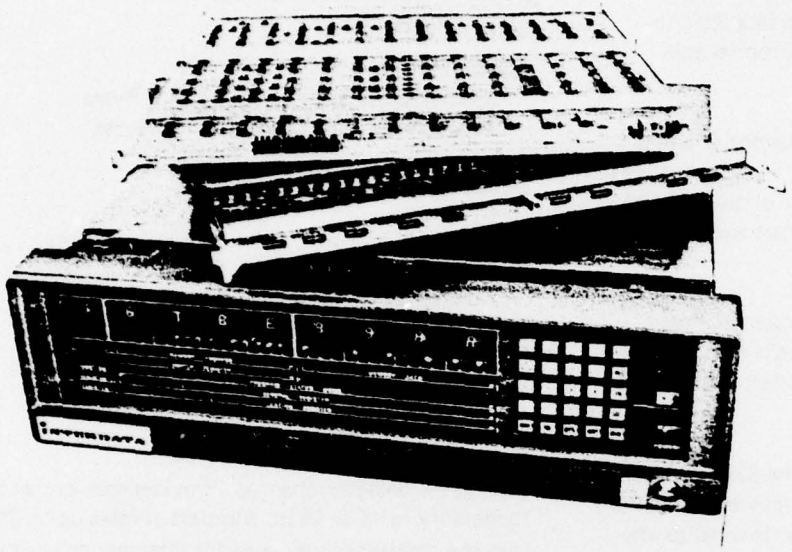
PROCESSORS

Model 6/16 Processor



PRODUCT DESCRIPTION

The Model 6/16 extends Interdata's 16-bit minicomputer technology by offering a powerful single-board processor with single-board memory as large as 64KB.

The memory is available in magnetic core with a cycle time of 1.0 microsecond, and MOS semiconductor with a cycle time of 600 nanoseconds.

Interdata's 16-bit hardware, software, and peripherals are upward compatible with Interdata's 32-bit products. This allows easy, simple expansion without affecting application software. Present software stands up. No expensive interface redesign is necessary. All presently used peripherals—discs, mag tapes, cassettes, printers, and A/D equipment—are compatible.

The Model 6/16 combines hardware versatility with complete software compatibility to offer the OEM and end user a flexible, expandable, and most economical minicomputer system.

FEATURES

- Advanced Architecture
  Task oriented 104-Instruction Set
  16 General Purpose Registers
  15 Index Registers
  Directly Addressable Memory to 64KB

- Built-In Reliability
  Printed circuit back panel for all interboard connections
  Thermal shock testing of all integrated circuits
  Vibration testing to 1.25 G's
  Burn In—52 hours at 50° C

- Field-Proven Software
  OS/16MT2—A real-time multi-tasking operating system
  Utilities—OS Edit, OS AIDS, OS Copy
  Languages—FORTRAN IV, FORTRAN V, Basic, MACROCAL
  CAL, CAL 16, COBOL

- Compatibility with Interdata's 32-bit products, application software, and peripherals.

SYSTEM ARCHITECTURE

The Model 6/16's inherently powerful third generation architecture, similar to the IBM 360/370 line, greatly simplifies system design, programming, and debugging.

The large task-oriented instruction set allows the programmer to concentrate on system programming instead of playing with tricky codes for such basic functions as exclusive OR, multiple shifts.

Sixteen general registers—15 of them index registers—reduce execution time and simplify program development, reduce overhead, and minimize housekeeping. Temporary results can be sorted for instant recall. And register-to-register operations cut programming steps while reducing execution time.

Up to 64 KB of directly addressable memory totally eliminates time consuming design problems caused by paging and indirect addressing. The architecture allows programmers to write straightforward, simple, in-line code for the Model 6/16.

INPUT/OUTPUT

The Model 6/16 Input/Output System handles up to 255 levels of interrupts. High speed devices can operate at up to 2,000,000 bytes per second over the optional Selector Channel, which makes use of Direct Memory Access. Medium and low speed devices are usually connected to the standard Multiplexor Channel.

Operation over the Selector or Multiplexor channels may be in the 8-bit parallel or 16-bit parallel mode. Both channels operate on a request-response basis for simple, reliable device-controller design. Multiplexor Channel devices are generally interrupt driven. Interrupts are automatically vectored for maximum machine efficiency and less software overhead.

Interdata offers a broad line of inexpensive peripherals for the Model 6/16 that are both program and interface compatible with all members of the Interdata family. Interdata also offers standard low cost interface modules to aid the user in designing special-purpose interfaces.

MEMORY

The Model 6/16 can accommodate one core or MOS semiconductor module of 8KB, 16KB, 32KB, or 64KB. All four module sizes are available with parity as an option.

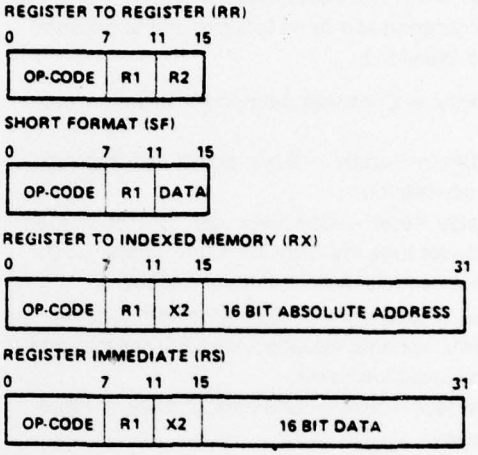
Each of the modules is contained on a single 15-inch printed circuit board and occupies a single memory slot. Core memory cycle time is 1.0 microsecond, semiconductor memory cycle time is 600 nanoseconds.

PHYSICAL CONFIGURATION

The Model 6/16 consists of one central processor printed circuit board, one memory module, and space for I/O device controllers. The standard chassis is a 7-inch rack mountable unit with 8 subassembly slots. A single subassembly slot can accommodate up to two optional boards.

The Model 6/16 is also available with a 14-inch dual chassis that provides 16 subassembly slots.

INSTRUCTION FORMAT



OP-CODE = HEXADECIMAL REPRESENTATION OF FUNCTION TO BE PERFORMED (ADD, MULTI.)
R1 = ANY ONE OF 16 G.P. REGISTERS AS A FIRST OPERAND.
R2 = ANY ONE OF 16 G.P. REGISTERS AS A SECOND OPERAND.
X2 = ANY ONE OF 15 INDEX REGISTERS AS AN INDEX VALUE (ADD TO APPARENT ADDRESS OR DATA FIELD TO OBTAIN TRUE VALUE OF ADDRESS OR DATA).

INSTRUCTION REPERTOIRE

The basic 104-instruction set provides big-machine capability that results in more time for applications programming and less worry about routine functions. While the 6/16 instruction formats are similar to those of the IBM 360/370, Interdata has added several classes of instructions to increase memory utilization efficiency. The instruction set provides both 16-bit and 32-bit formats and permits operation between any two general registers (RR), a general register and any memory location (RX), a general register and a 16-bit data constant carried in the primary instruction word (RI), or a general register and 4-bit data constant (SF). Fixed-point multiply/divide hardware increases the number of instructions to 110.

The Model 6/16 includes a complete set of arithmetic and logical instructions. A complete set of conditional branch instructions permits branching to any location in memory without the use of skips. A full set of byte processing instructions simplifies handling of byte strings and pro-

vides for more efficient use of available memory. The input/output instructions permit operations between peripheral devices and general registers or between devices and memory. In addition to enabling programmers to write programs in as few instructions as possible, the 6/16's straightforward, efficient instruction set greatly simplifies the debugging and documentation problems associated with machines with smaller instruction sets.

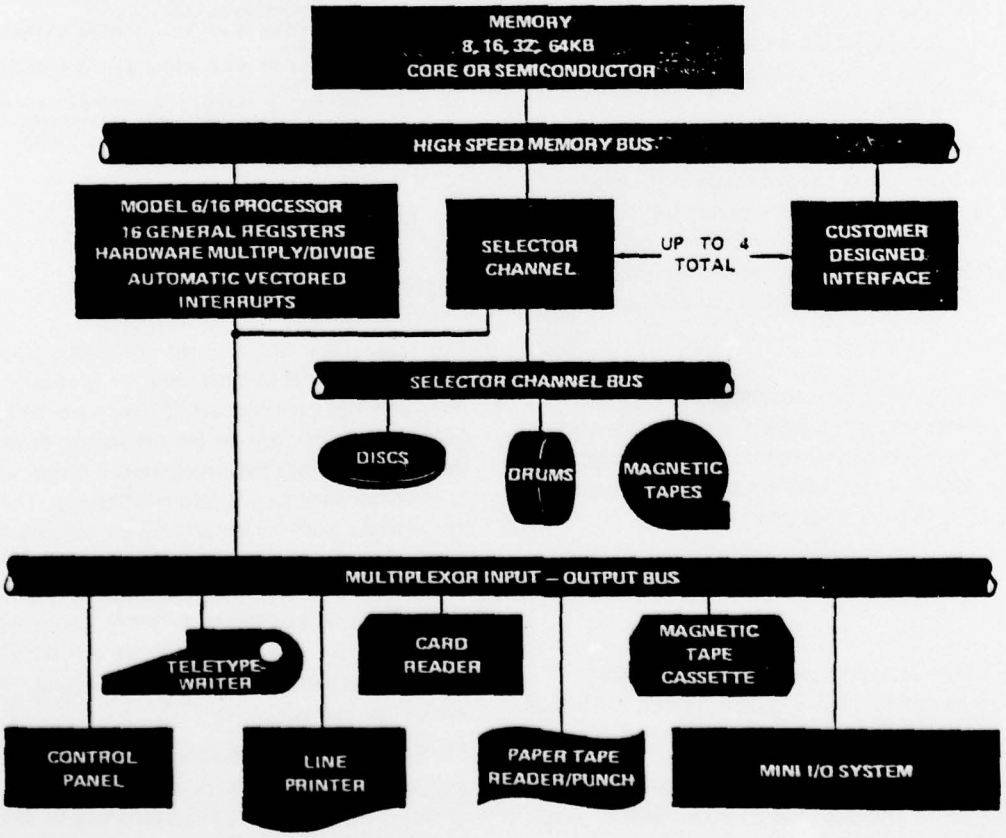
OPTIONS

Model 6/16 options provide extensive flexibility so that the hardware configuration can be tailored to the application and easily field expanded.

- Memory Parity – Complete data and instruction protection.
- Power Fail/Auto Restart – Early power fail interrupt and power-up interrupt.
- Binary Display Panel – Complete user control of the system. Includes long life Light Emitting Diode (LED) binary readout and hexadecimal input keyboard.
- Hexadecimal Display Panel – Complete user control of the system. Includes Hexadecimal LED readout and Hexadecimal input keyboard.
- Display Interface – Interfaces Binary Display or Hexadecimal display.
- Automatic Load Option – Simple, single-switch bootstrap load capability. Can be preprogrammed with OS/16MT2 loader or can be used with a custom designed program.
- Turnkey Console – Switch control for Model 6/16 power, initialize, and execution.
- Signed Multiply/Divide – Hardware execution of 16-bit fixed point signed multiply and divide and unsigned multiply.
- Selector Channel – For high-speed I/O requirements provides completely autonomous block transfers on a cycle stealing basis for high speed I/O.
- Stretch 32 – Field updates a Model 6/16 processor to a software and I/O compatible 7/32 processor. The expanded system is capable of directly addressing one megabyte of memory and executing a full complement of 32-bit fullword instructions.

BUILT-IN RELIABILITY

The Model 6/16 uses the latest techniques in logic design, solid state technology, mechanical packaging, and manufacturing testing to ensure maximum hardware reliability and to minimize downtime. A printed circuit back panel provides all interboard connections. Individual logic boards are connected to the back panel with in-line connectors, eliminating the contact problems associated with edge connectors.



UP TO 255 DEVICES IN SYSTEM

PACKAGING

Model 6/16 packaging is consistent with Interdata standards of ruggedness, durability, and reliability. Interboard connections are military-type pin and receptable connectors for sure, positive connection. Separately mounted power supplies, readily accessible test points and fuses, and plug-in modules mean fewer failures and less time for repairs. Interdata's testing includes thermal shock testing of all integrated circuits. The Model 6/16 is vibration tested at 1.25 G's while running diagnostic programs. Finally, all processors are run for 52 hours at 50°C – the quality is burned in.

OPERATING SYSTEMS AND DEVELOPMENT SOFTWARE

Interdata provides a comprehensive family of compatible operating systems and utility programs as off-the-shelf packages. All software is fully warranted and is supported by both field and home office staffs. Software includes:

- OS/16 MT2—Real-time based multi-tasking multi-programming operating system.
- FORTRAN compilers—Extended FORTRAN IV and FORTRAN V.
- OS AIDS—Interactive debug program.
- CAL—A common assembly language for all Interdata processors.
- CAL 16—for 16 Bit Processors only.
- BASIC interpreter—Superset of Dartmouth standard.
- OS Edit – Text editor.

A complete line of utility programs is available. And the Interdata users group, INTERCHANGE, has an extensive software library.

A large array of reliable peripherals and interfaces reduces risk and development costs. The Interdata peripheral family includes a complete range of magnetic tapes, discs, card and paper tape equipment, CRT displays, printers, analog and digital converters, data acquisition equipment, communications access methods, and IBM 360 interfaces.

COMPATIBILITY

The Model 6/16 is completely hardware and software compatible with the entire Interdata 16-bit line, as well as being upward compatible through the 32-bit series. Interdata's emphasis on design compatibility results specifically in investment protection and broader applications capability at less cost to the OEM and end user. OS/16 MT2, for example, is a subset of the 32-bit operating system, OS/32 MT.

SPECIFICATIONS

Technology
  Processor T^2L-MSI–LSI
  ROM Bipolar (60 ns access time)
Data Word Length—8, 16, 32 bits
Instruction Word Length—16, 32 bits
Number of Basic Instructions—104
  With Multiply/Divide Option—110
Fixed Point Arithmetic—2's Complement
Hardware Accumulators—16
Hardware Index Registers—15
Address Modes—Direct and Indexed

Memory
Core Memory Cycle Time—1.0 usec
MOS Semiconductor Memory Cycle Line—600 nanoseconds
Memory Capacity—64K bytes
Memory Increments—8KB, 16KB, 32KB, or 64KB

Typical Instruction Execution Timing

	Semiconductor	Core
Register-to-Register	.90 usec	1.0 usec
Memory Reference	2.40 usec	3.0 usec
Immediate	1.50 usec	2.0 usec

Input/Output
High Speed DMA Channels—Four standard.
Maximum Selector Channel transfer rate: 2MByte
Input/Output System—8 or 16-bit word lengths
255 priority interrupt levels
Programmed I/O Loop Rate—66KB
Interrupt Response Time—7.75 usec
(including storage of Current Program Status Word and generation of New Program Status Word)
I/O Bus Levels—Ground and +5 volts
Hardware I/O Time Out—14 usec (approx.)

Environmental
Operating Temperature—0°C to 50°C
Storage Temperature Range—55°C to 85°C
Vibration—0 to 55 CPS at 1.25G
Relative Humidity—to 90% without condensation

Packaging
Chassis Dimensions—
  7 inches by 19 inches by 26 inches RETMA
  14 inches by 19 inches by 26 inches RETMA
Power Supply Dimensions—
  7 inches by 19 inches by 9 inches RETMA
Weight with Power Supply—
  Single Chassis, 50 pounds
  Double Chassis, 70 pounds
Primary Power—115 or 230 VAC ± 10%, 47 to 63 Hz
  Single Chassis—3.6 amp maximum
  Double Chassis—6.0 amp maximum

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